GSENSE1517BSI

15µm, 16.8MP Scientific CMOS Image Sensor

Datasheet V 0.3.1

Features

- Large format sensor with frame rate up to 4fps
- 92% Peak QE @450nm
- 79.6dB from a single image and 95.3dB from dual gain HDR
- Low dark current: 0.1e$^-$/s/pix @ -30ºC
- Anti-glowing
- On-chip 12-bit and 14-bit column-parallel ADC
- SiC with Al_2O_3 IPGA ceramic package

Applications

- Astronomy Application
- Space Situational Awareness (SSA)
- Physical sciences research

Description

GSENSE1517BSI is a 4116 x 4100 (16.8 MP) resolution scientific image sensor with high-performance 15 x 15 μm^2 pixels, a large 61.74 x 61.50 mm imaging area, peak QE of 92% and minimum read noise 1.2 e$^-$.

The sensor utilizes dual-gain HDR and both 12-bit and 14-bit ADCs to achieve a variety of imaging modes. Both 12-bit HDR and 14-bit STD are supported at up to 4 fps utilizing 10 pairs of LVDS working at 420 Mbps each. In 12-bit dual-gain HDR mode, an intra-scene dynamic range over 95.3 dB is achieved with 70 ke$^-$ full well capacity and 1.2 e$^-$ readout noise. In 14-bit STD mode, either the LG or HG signal can be utilized. Using the HG signal, read noise is 1.5 e$^-$ and a dynamic range of 79.6 dB is achieved. Using the LG signal, the maximum full well capacity of 70 ke$^-$.

GSENSE1517BSI is assembled in a high-end SiC package designed such that the dead space at 3x package sides is minimized for mosaic tiling. The thermal expansion of SiC is close to that of the silicon die, providing mechanical stability over the sensor's full operating range from -40℃ to 50℃.

Specifications

The table below lists the key specifications of GSENSE1517BSI. All the parameters are specified at room temperature unless otherwise noted.

Parameter	Value
Photosensitive area	61.74 mm x 61.50 mm
Pixel size	15 μm x 15 μm
Active resolution	4116(H) x 4100 (V)
Shutter type	Rolling shutter
Full well capacity	70ke$^-$@ 12-bit HDR 70ke$^-$@ 14-bit LG 14.4ke$^-$@ 14-bit HG
Temporal noise	1.2e$^-$@ 12-bit HDR 10.9e$^-$@ 14-bit LG 1.5e$^-$@ 14-bit HG
Dynamic range	95.3dB @ 12bit HDR 79.6dB @ 14-bit HG 76.1dB @ 14-bit LG
Clock rate	420 MHz
Peak QE	92%@450nm
Dark current	0.1e$^-$/s/pix @ -30℃
Frame rate	4fps@12bit HDR &14bit
Data rate	Max.4.2 Gbps
Output format	10 pairs of LVDS data channels 1 pair of DDR channel
Supply voltage	Analog 3.3V Digital 1.55V IO 1.8V
Power consumption	<1.0 W
Chroma	Mono
Package	SiC with 144-pin Al_2O_3 IPGA ceramic package

Revision History

Version	Date(dd/mm/yyyy)	Comment
V0.1	14/03/2024	First release, preliminary version for hardware design
V0.1.1	09/04/2024	1. Modify section of “Power On/Off Sequence” 2. Add 100Ω resistance between CLKP_IN and CLKN_IN in Figure 23 3. Add chapters related to FPGA design.
V0.1.2	14/05/2024	1. Add Figure 1 2. Update Figure 2 and Figure 3 3. Update Figure 50
V0.1.3	15/08/2024	Update office location
V0.3.0	17/12/2024	1. Update section of “Features”, “Description” and Specifications, add section of “Applications” 2. Update section of “Absolute Maximum Ratings”, “Package Outline”, “Optical Center” and “Pixel Arrangement” 3. Update section of “Pin Description” and “DC Characteristics” 4. Update Table 4 and Table 5 5. Update section of “Power Consumption” 6. Add section of “Image Sensor Characteristics” 7. Update Table 11 8. Update section of “Array Supply Connections” and “Bias and Reference Pin Connections” 9. Detele 100Ω resistance between CLKP_IN and CLKN_IN in Figure 23 10. Update section of “Power On/Off Sequence”, “Reset Sequence” and “Register Communication Timing” 11. Modified dummy address 12. Update section of “Frame Time Settings” and “Exposure Time Settings” 13. Update section of “Timing of Control Signals” 14. Update Table 18 and Table 21, update section of “Data Receiving” 15. Update Figure 56 and Figure 57 16. Delete section of “PGA Gain Adjustment” and “Analog Temperature Diode” 17. Update section of “Test Image” 18. Add section of “Blemish Specification” and “Storage Condition, Handling and Soldering”
V0.3.1	13/01/2025	1. Update sensor spec in “Specifications” and “Image Sensor Characteristics” 2. Add “Product Order Information” 3. Update Figure 3

		4. Moidify description of pin G11, H10 and H18 in Table 2 5. Update Figure 21 6. Modify the description in section of “Register Communication Timing” 7. Update section of “Windowing Operation”

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	VDDA	-0.3 to +3.63	V	
Supply Voltage	VDDA_BIAS	-0.3 to +3.63	V	
Supply Voltage	VDDIO	-0.3 to +3.63	V	
Supply Voltage	VDDD	-0.3 to +1.65	V	
Supply Voltage	VDDAD	-0.3 to +1.65	V	
Pixel Supply Voltage	VDDSF	-0.3 to +3.63	V	
Pixel Supply Voltage	VDDCH	-0.3 to +3.63	V	
Pixel Supply Voltage	VRH	-0.3 to +3.63	V	
Pixel Supply Voltage	VDRH	-0.3 to +3.63	V	
Pixel Supply Voltage	VTXH	-0.3 to +3.63	V	
Pixel Supply Voltage	VSH	-0.3 to +3.63	V	
Pixel Supply Voltage	VFIXH	-0.3 to +3.63	V	
Pixel Supply Voltage	VDDCL	-0.3 to +3.63	V	
Pixel Supply Voltage	VRL	-2.0 to 0.3	V	
Pixel Supply Voltage	VDRL	-0.3 to +3.63	V	
Pixel Supply Voltage	VTXL	-2.0 to 0.3	V	
Pixel Supply Voltage	VSL	-2.0 to 0.3	V	
Pixel Supply Voltage	VFIXL	-0.3 to +3.63	V	
Analog reference voltage	VREF	-0.3 to +3.63	V	
Analog reference voltage	VRAMP_PC	-0.3 to +3.63	V	
Analog reference voltage	VRAMP_INIT	-0.3 to +3.63	V	
Input Voltage	VI	-0.3 to VDDIO+0.3	V	NOT exceed +3.63
Output Voltage	VO	-0.3 to VDDIO+0.3	V	NOT exceed +3.63
Operation Temperature	Topr	-40 to +50	°C	Junction temperature
Storage Temperature	Tstg	T.B.D	°C	Environment temperature

Content

Package Outline

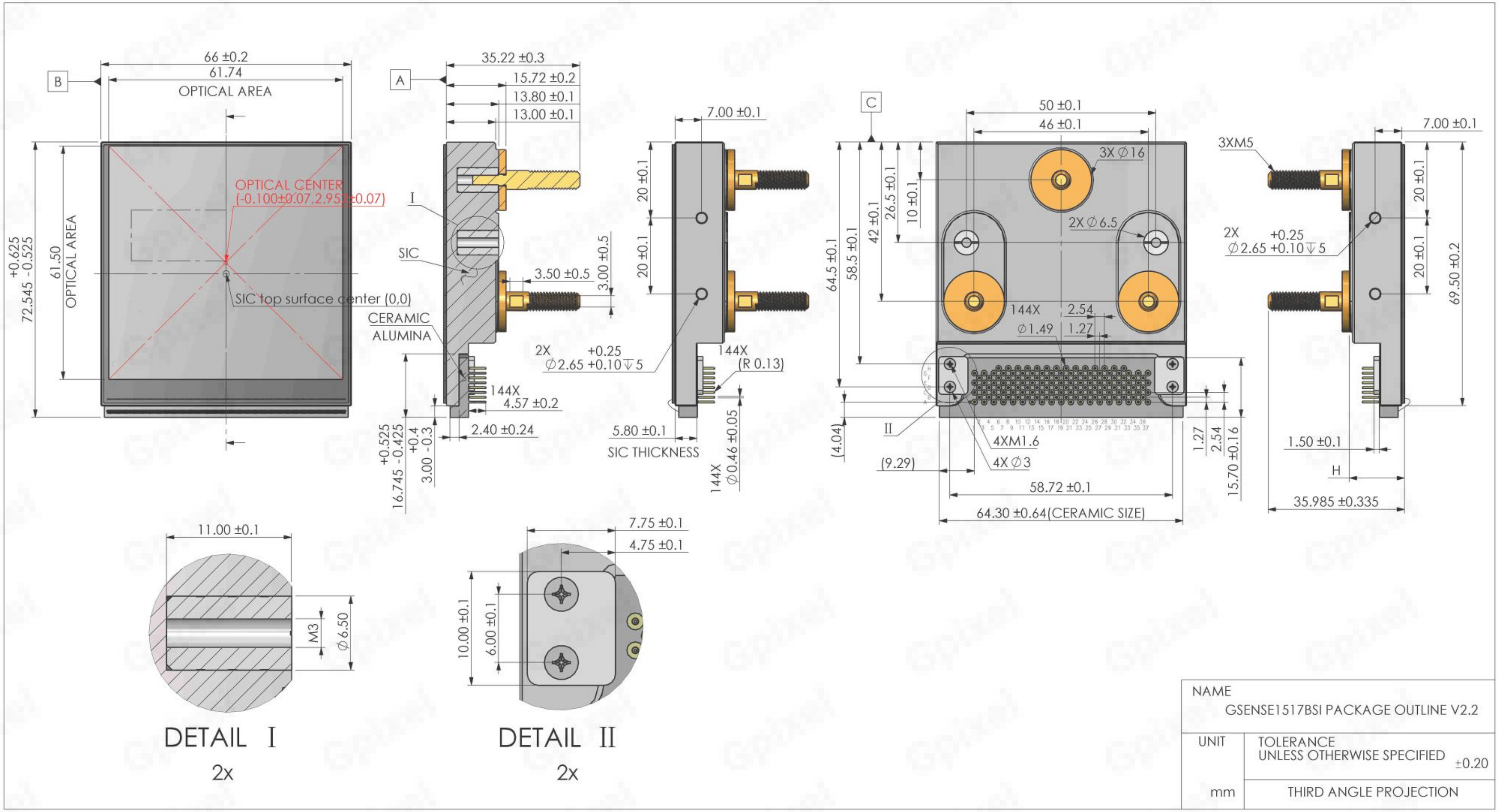


Figure 1: Package outline

Note:

1. The center of the optical sensitive area is at (-0.100 ± 0.07mm, 2.952± 0.07mm) relative to the center of the die attach surface of the SiC-base.
2. The deviation of the die center relative to the die attach surface center of the SiC-base is ± 0.07mm. The rotation angle of the die relative to the die attach surface edge of the SiC-base is ± 0.3°. The tilt of the die relative to the die attach surface of the SiC-base is less than 0.16 mm.
3. The distance from the die surface to the mounting surface of the SiC-base is 14.565 ± 0.135 mm (H).
4. The thermal conductivity of the SiC-base is 121 W/(m·K).
5. The thermal expansion coefficient of the SiC-base is 4 x 10^{-6}/℃ from 0 to 1200℃.

Optical Center

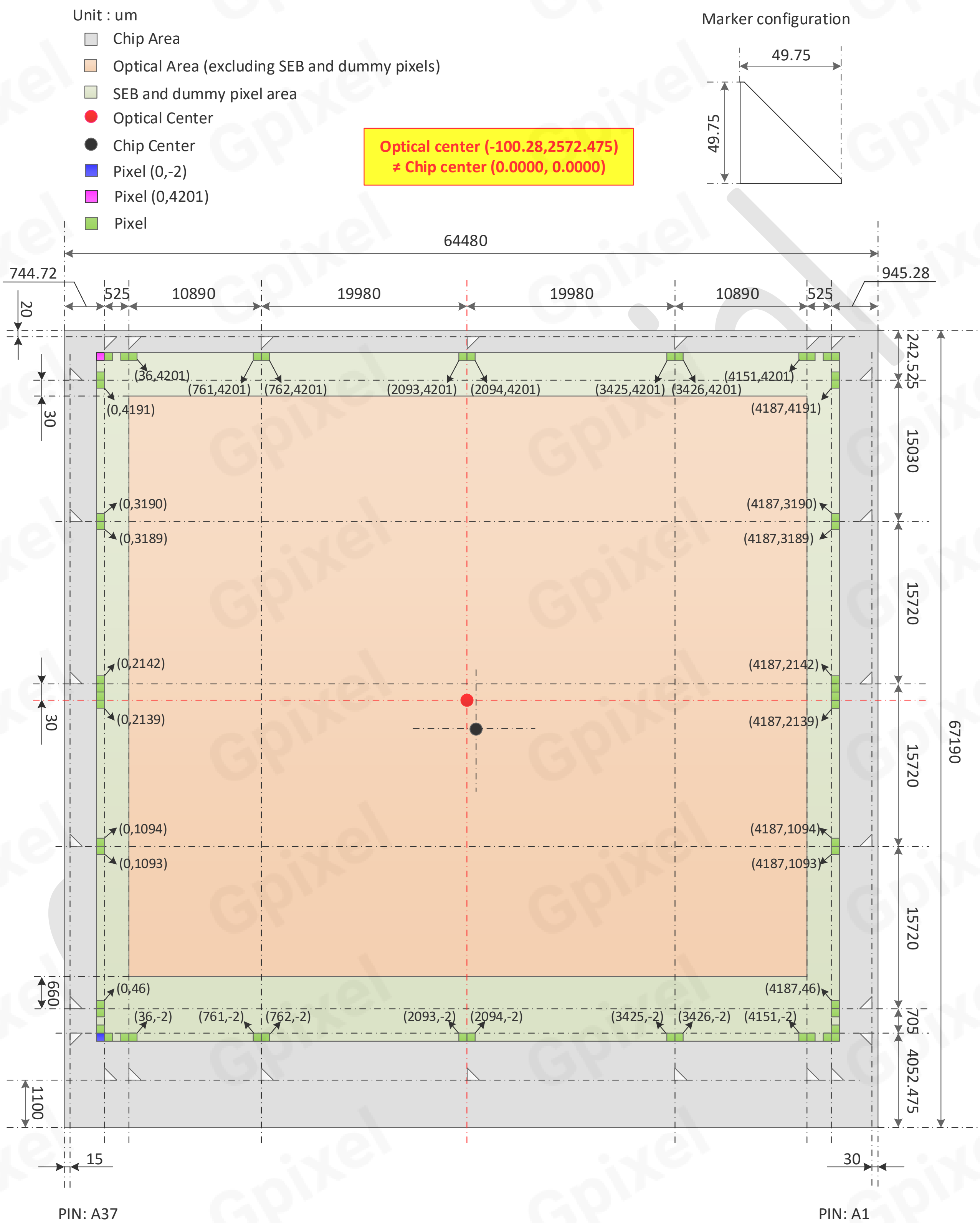


Figure 2: Optical center(top view)

Pixel Arrangement

The total readable pixel array is 4188(H) x 4192(V), including 36 columns of selectable electrical black(SEB) pixels at the left and right of the active array respectively. This SEB columns can be enabled through SPI registers setting shown in Table 1. If SEB pixels are enabled, the input of readout circuits for SEB columns will be tied to a stable reference voltage, generating dark outputs. The behavior of SEB pixels will be the same as active pixels if they are disabled.

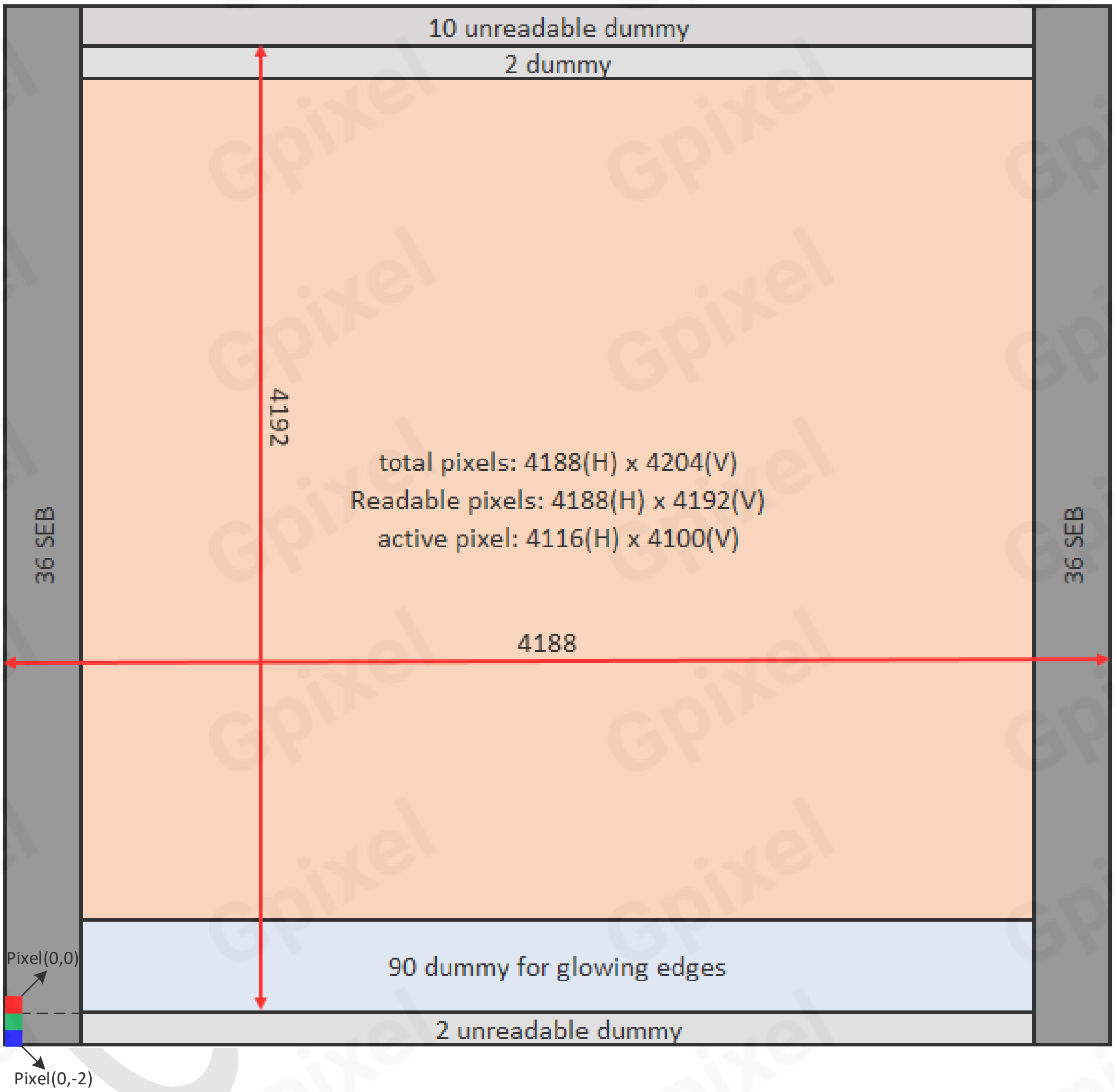


Figure 3: Pixel arrangement(top view)

Table 1: SEB configuration

Address (H)	Bit	Register Name	Description
13	7	REG_EB_R_EN	0：active pixels 1：EB pixels
25	0	REG_EB_L_EN	0：active pixels 1：EB pixels

Internal Block Diagram and Pin Description

Internal Block Diagram

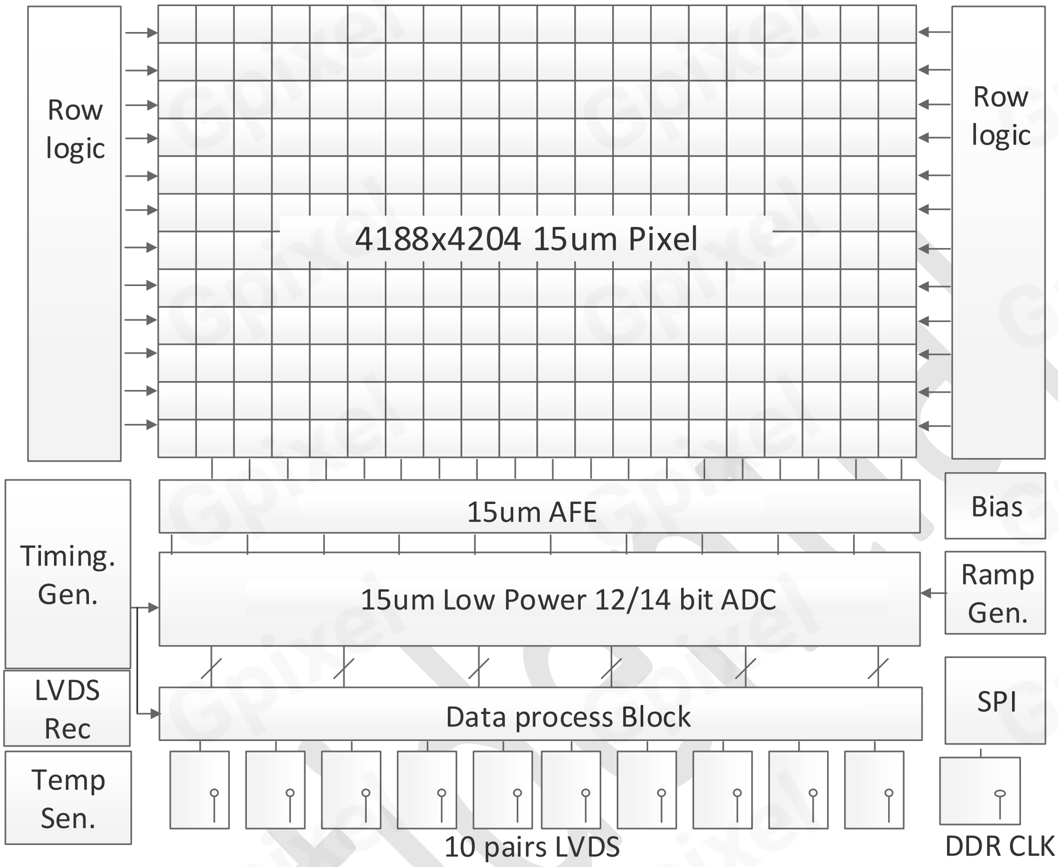


Figure 4: Block diagram

Pin Description

Table 2: Pin description

No.	Pin No.	I/O	Symbol	Description	Type
1	A1	Power	VDRL	Supply of pixel control signal (current sink)	Supply
2	A3	Power	VDDAD	Digital supply	Supply
3	A5	Power	VDDSF	Pixel array supply	Supply
4	A7	Power	VDDAD	Digital supply	Supply
5	A9	Power	VDDD	Digital supply	Supply
6	A11	Power	VDDAD	Digital supply	Supply
7	A13	Power	VDDA	Analog supply	Supply
8	A15	Power	VDDAD	Digital supply	Supply
9	A17	Power	VDDIO	I/O ring supply	Supply
10	A19	Power	VDDD	Digital supply	Supply
11	A21	Power	VDDCH	Supply of pixel control signal	Supply
12	A23	Power	VDDAD	Digital supply	Supply
13	A25	Power	VDDA	Analog supply	Supply
14	A27	Power	VDDAD	Digital supply	Supply
15	A29	Power	VDDD	Digital supply	Supply
16	A31	Power	VDDAD	Digital supply	Supply
17	A33	Power	VDDSF	Pixel array supply	Supply
18	A35	Power	VDDAD	Digital supply	Supply
19	A37	I	CLKN_IN	LVDS receiver input clock negative	LVDS input
20	B2	GND	GNDD	Digital ground	Ground
21	B4	GND	GNDAD	Digital ground	Ground
22	B6	GND	GNDA	Analog ground	Ground
23	B8	GND	GNDAD	Digital ground	Ground
24	B10	GND	GNDD	Digital ground	Ground
25	B12	GND	GNDAD	Digital ground	Ground
26	B14	GND	GNDA	Analog ground	Ground
27	B16	GND	GNDAD	Digital ground	Ground
28	B18	GND	GNDD	Digital ground	Ground
29	B20	Power	VDDCL	Supply of pixel control signal (current sink)	Supply
30	B22	GND	GNDAD	Digital ground	Ground
31	B24	GND	GNDA	Analog ground	Ground
32	B26	GND	GNDAD	Digital ground	Ground
33	B28	GND	GNDD	Digital ground	Ground
34	B30	GND	GNDAD	Digital ground	Ground
35	B32	GND	GNDA	Analog ground	Ground
36	B34	GND	GNDAD	Digital ground	Ground
37	B36	Power	VDDD	Digital supply	Supply
38	C1	Power	VDDD	Digital supply	Supply

39	C3	O	OUTN<9>	LVDS negative output channel 9	LVDS output
40	C5	O	CLKN_OUT	LVDS clock negative output	LVDS output
41	C7	O	OUTN<8>	LVDS negative output channel 8	LVDS output
42	C9	I	DEC<4>	Digital control signal	Digital input
43	C11	I	DEC<1>	Digital control signal	Digital input
44	C13	O	OUTN<7>	LVDS negative output channel 7	LVDS output
45	C15	O	OUTN<6>	LVDS negative output channel 6	LVDS output
46	C17	O	OUTN<5>	LVDS negative output channel 5	LVDS output
47	C19	I	RST	Digital control signal	Digital input
48	C21	O	OUTN<4>	LVDS negative output channel 4	LVDS output
49	C23	O	OUTN<3>	LVDS negative output channel 3	LVDS output
50	C25	O	OUTN<2>	LVDS negative output channel 2	LVDS output
51	C27	O	CLK_PIX<0>	Digital test pin0	Digital output
52	C29	I	HG_LG_SW	Digital control signal	Digital input
53	C31	O	OUTN<1>	LVDS negative output channel 1	LVDS output
54	C33	O	OUTN<0>	LVDS negative output channel 0	LVDS output
55	C35	GND	GNDD	Digital ground	Ground
56	C37	I	CLKP_IN	LVDS receiver input clock positive	LVDS input
57	D2	GND	GNDA	Analog ground	Ground
58	D4	O	OUTP<9>	LVDS positive output channel 9	LVDS output
59	D6	O	CLKP_OUT	LVDS clock positive output	LVDS output
60	D8	O	OUTP<8>	LVDS positive output channel 8	LVDS output
61	D10	I	DEC<5>	Digital control signal	Digital input
62	D12	I	DEC<0>	Digital control signal	Digital input
63	D14	O	OUTP<7>	LVDS positive output channel 7	LVDS output
64	D16	O	OUTP<6>	LVDS positive output channel 6	LVDS output
65	D18	O	OUTP<5>	LVDS positive output channel 5	LVDS output
66	D20	O	OUTP<4>	LVDS positive output channel 4	LVDS output
67	D22	O	OUTP<3>	LVDS positive output channel 3	LVDS output
68	D24	O	OUTP<2>	LVDS positive output channel 2	LVDS output
69	D26	I	VPC_SW	Digital control signal	Digital input
70	D28	I	SYNC	Digital control signal	Digital input
71	D30	O	OUTP<1>	LVDS positive output channel 1	LVDS output
72	D32	O	OUTP<0>	LVDS positive output channel 0	LVDS output
73	D34	I	RAMP_INIT	Digital control signal	Digital input
74	D36	GND	GNDA	Analog ground	Ground
75	E1	I/O	RES_NODE_N	Connected to RES_NODE_P through a 12.4KΩ resistor	Analog input/output
76	E3	I	DEC<12>	Digital control signal	Digital input
77	E5	I	DEC<11>	Digital control signal	Digital input
78	E7	I	DEC<8>	Digital control signal	Digital input
79	E9	I	DEC<6>	Digital control signal	Digital input

80	E11	I	DEC<2>	Digital control signal	Digital input
81	E13	O	CLK_PIX<1>	Digital test pin1	Digital output
82	E15	I	VDDC	Digital control signal	Digital input
83	E17	I	TX	Digital control signal	Digital input
84	E19	I	SEL	Digital control signal	Digital input
85	E21	I	SPI_SYNC	SPI sync control signal	Digital input
86	E23	I	LP_RST_N	Digital control signal	Digital input
87	E25	I	FRAME_CTRL	Digital control signal	Digital input
88	E27	I	CLK_RST_N	Clock reset signal	Digital input
89	E29	I	VTZ	Digital control signal	Digital input
90	E31	I	CPC	Digital control signal	Digital input
91	E33	I	RAMP_PC	Digital control signal	Digital input
92	E35	I	BIAS_SAMP	Digital control signal	Digital input
93	E37	I/O	VPCL	Decouple with 10uF to GNDA	Bias
94	F2	Power	VDDA	Analog supply	Supply
95	F4	O	SPI_OUT	SPI output	Digital output
96	F6	I	DEC<10>	Digital control signal	Digital input
97	F8	I	DEC<9>	Digital control signal	Digital input
98	F10	I	DEC<3>	Digital control signal	Digital input
99	F12	I	DEFECT_CLK	Digital control signal	Digital input
100	F14	I	DEFECT_IN	Digital control signal	Digital input
101	F16	I	HDR	Digital control signal	Digital input
102	F18	I	SPI_CLK	SPI input clock	Digital input
103	F20	I	SPI_IN	SPI input data	Digital input
104	F22	I	SYS_RST_N	System reset signal	Digital input
105	F24	I	LP_RDL_N	Digital control signal	Digital input
106	F26	I	TRAIN	Digital control signal	Digital input
107	F28	I	RAMP	Digital control signal	Digital input
108	F30	I	BLS_CLIP	Digital control signal	Digital input
109	F32	I	DP_HG_LG_SW	Digital control signal	Digital input
110	F34	I	PGA_INIT	Digital control signal	Digital input
111	F36	Power	VDDA	Analog supply	Supply
112	G1	I/O	RES_NODE_P	Connected to RES_NODE_N through a 12.4KΩ resistor	Analog input/output
113	G3	I/O	VCBP	Decouple with 100nF to VDDA_BIAS	Bias
114	G5	I/O	TBD<2>	N.C	N.C
115	G7	Power	VDDA_BIAS	Analog bias supply	Supply
116	G9	I	DEC<7>	Digital control signal	Digital input
117	G11	I/O	VRAMP_PC	Voltage reference of analog chain (current sink and source)	Voltage reference
118	G13	Power	VFIXL	Supply of pixel control signal (current sink)	Supply

119	G15	I/O	VDP<1>	Connected to GNDA	Analog input/output
120	G17	Power	VSH	Supply of pixel control signal	Supply
121	G19	Power	VTXH	Supply of pixel control signal	Supply
122	G21	Power	VRL	Supply of pixel control signal (current sink)	Supply
123	G23	I/O	VCASN_RAMP	Decouple with 100nF to GNDA	Bias
124	G25	I	LP_RDS_N	Digital control signal	Digital input
125	G27	Power	VFIXH	Supply of pixel control signal	Supply
126	G29	I/O	VDP<0>	Connected to GNDA	Analog input/output
127	G31	Power	VRH	Supply of pixel control signal	Supply
128	G33	I/O	VPCH	Decouple with 10uF to GNDA	Bias
129	G35	Power	VTXL	Supply of pixel control signal (current sink)	Supply
130	G37	I/O	ANA_TBD	N.C	N.C
131	H6	I/O	VBG	Decouple with 100nF to GNDA	Bias
132	H8	Power	VSL	Supply of pixel control signal (current sink)	Supply
133	H10	I/O	VRAMP_INIT	Voltage reference of analog chain (current sink and source)	Voltage reference
134	H12	O	TANA<0>	N.C	N.C
135	H14	I/O	VDN<1>	Connected to GNDA	Analog input/output
136	H16	I/O	TBD<1>	N.C	N.C
137	H18	I/O	VREF	Voltage reference of analog chain (current sink and source)	Voltage reference
138	H20	I/O	VLBP	Decouple with 100nF to VDDA_BIAS	Bias
139	H22	I/O	VCMDP_RAMP	Decouple with 100nF to VDDA_BIAS	Bias
140	H24	Power	VDRH	Supply of pixel control signal	Supply
141	H26	O	TANA<1>	N.C	N.C
142	H28	I/O	VDN<0>	Connected to GNDA	Analog input/output
143	H30	I/O	TBD<0>	N.C	N.C
144	H32	I/O	VPBP	Decouple with 100nF to VDDA_BIAS	Bias

Note:

Electrical Characteristics

DC Characteristics

Table 3: DC characteristics

Item	Pins	Symbol	Min.	Typ.	Max.	Unit	Note
Analog supply	VDDA		3.25	3.3	3.35	V	
	VDDA_BIAS		3.25	3.3	3.35	V	
Analog reference voltage	VREF		1.72	1.75	1.78	V	1
	VRAMP_PC		2.57	2.6	2.63	V	1
	VRAMP_INIT		2.77	2.8	2.83	V	1
Digital supply	VDDD		1.52	1.55	1.58	V	
	VDDAD		1.52	1.55	1.58	V	
	VDDIO		1.7	1.8	3.3	V	
Pixel supply	VDDSF		3.25	3.3	3.35	V	
	VDDCH		2.95	3.0	3.05	V	
	VDDCL		1.75	1.8	1.85	V	1
	VRH		3.45	3.5	3.55	V	1
	VRL		0	0	0	V	2
	VSH		3.25	3.3	3.35	V	1
	VSL		0	0	0	V	2
	VDRH		3.45	3.5	3.55	V	1
	VDRL		0	0	0	V	2
	VTXH		2.75	2.8	2.85	V	1
	VTXL		-0.23	-0.2	-0.17	V	1
	VFIXH		3.25	3.3	3.35	V	1
	VFIXL		0	0	0	V	2
Digital input	All digital input pins	VIH	VDDIO-0.3	VDDIO	VDDIO+0.3	V	
		VIL	0	0	0.3	V	
	CLKP_IN	VCM		1.25		V	
	CLKN_IN	VOD		0.35		V	
Digital output	CLKN_OUT CLKP_OUT	V_{OCM}		1.0		V	
	OUTN<10:0> OUTP<10:0>	V_{ODIFF}		0.3		V	
	CLK_PIX<1:0>	VOH	VDDIO-0.3	VDDIO	VDDIO+0.3	V	
	SPI_OUT	VOL	0	0	0.3		

Note:

1. These supplies are designed with current source and drain ability of around 50mA on Gpixel evaluation board.
2. VSL, VRL, VDRL and VFIXL are shorted to GND on Gpixel evaluation board.

3. The characterization results are measured with the typical values of all supplies and refernces in the above table.

AC Characteristics

1. Digital input control signal waveform diagram

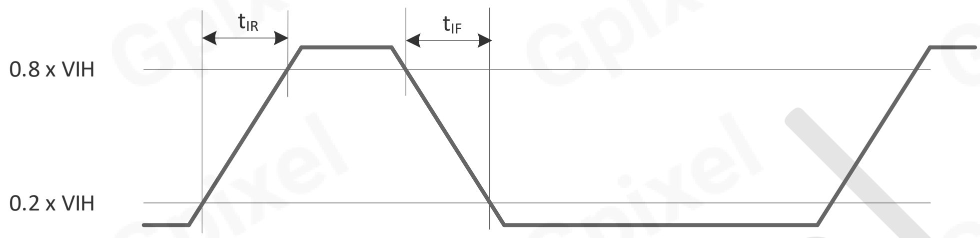


Figure 5: AC digital input control signal

Table 4: AC characteristics for digital input control signals

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Control signal rising edge	t_{IR}	—	1.7	—	ns	Define with 0.2 x VIH and 0.8 x VIH
Control signal falling edge	t_{IF}	—	1.2	—	ns	Define with 0.2 x VIH and 0.8 x VIH

2. Digital Output Signal waveform diagram

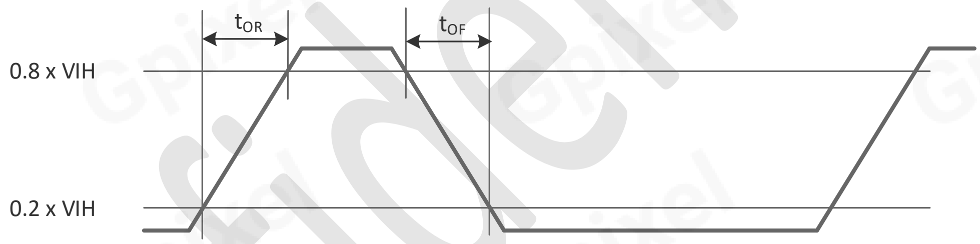


Figure 6: AC digital output control signal

Table 5: AC characteristics for digital input control signal

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Digital output signal rising edge	t_{OR}	—	0.9	—	ns	Define with 0.2 x VIH and 0.8 x VIH
Digital output signal falling edge	t_{OF}	—	0.8	—	ns	Define with 0.2 x VIH and 0.8 x VIH

Note:

Output load capacitance < 18pF.

3. LVDS Driver Output

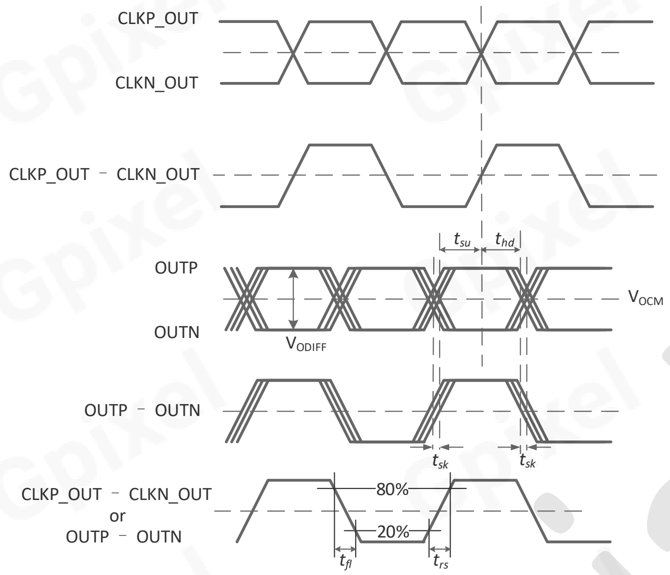


Figure 7: LVDS driver output

Table 6: LVDS driver output

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock Duty Cycle		40	50	60	%	DDR clock 210MHz
Data setup time	t_{su}	T.B.D	—	—	ps	Data rate 420Mbps
Data hold time	t_{hd}	T.B.D	—	—	ps	Data rate 420Mbps
Data skew time	t_{sk}	—	—	T.B.D	ps	Data rate 420Mbps
Data rising time	t_{rs}	—	497.5	—	ps	Simulated value with load 8pF capacitance
Data falling time	t_{fl}	—	491.1	—	ps	Simulated value with load 8pF capacitance
Differential output voltage	V_{ODIFF}	T.B.D	300	—	mV	
Output Common mode voltage	V_{OCM}	—	1.0	—	V	

Note:

1. The same AC characteristics applies for data channel and clock channel.
2. Output load capacitance < 8pF.

Power Consumption

The power consumption is listed in Table 7.

Table 7: Power consumption

Supply source	Typical voltage (V)	Average current (mA)	Peak current (mA)	Average power consumption (mW)
VDDA	3.3	93	104	360.9
VDDA_BIAS	3.3	<10	<10	
VDDD	1.55	175	179	271.25
VDDAD	1.55	121	132	187.55
VDDSF	3.3	25	44	82.5
VDDCH	3.0	<10	<10	
VDDIO	1.8	<10	<10	
VRH	3.5	<10	<10	
VDRH	3.5	<10	<10	
VTXH	2.8	<10	<10	
VSH	3.3	<10	<10	
VFIXH	3.3	<10	<10	
VDDCL	1.8	<10	<10	
VRL	0	<10	<10	
VDRL	0	<10	<10	
VTXL	-0.2	<10	<10	
VSL	0	<10	<10	
VFIXL	0	<10	<10	
VREF	1.75	<10	<10	
VRAMP_PC	2.6	<10	<10	
VRAMP_INIT	2.8	<10	<10	
Total Power consumption (mW)				848.2

Image Sensor Characteristics

Key Specification

Table 8: Key performance for 14-bit STD mode

Item	14-bit STD LG			14-bit STD HG			Unit	Note
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Conversion factor		0.18			1.03		DN/e^-	
Full well capacity		70			14.4		ke^-	1
Non-linearity error		0.5			0.5		%	2
Max. SNR		48.4			41.5		dB	3
Temporal dark noise		10.9			1.5		e^-	
Dynamic range		76.1			79.6		dB	4
Peak QE @ 450nm		92.6					%	5
Sensitivity @ 450nm		4.72 x10^8					e^-/ ((W/m^2)·s)	
Dark current					0.1		e^-/s/pix	6
DSNU		38.1			5.5		e^-	7
PRNU		0.9			1.0		%	7

Table 9: Key performance for 12-bit HDR mode

Item	12-bit HDR LG			12-bit HDR HG			Unit	Note
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Conversion factor		0.044			1.31		DN/e^-	
Full well capacity		70			2.8		ke^-	1
Non-linearity error		0.4			0.7		%	2
Max. SNR		48.4			34.4		dB	3
Temporal dark noise		18.6			1.2		e^-	
Dynamic range		71.5			67.3		dB	4
Dynamic range (HDR image)	95.3						dB	4
DSNU		49.3			3.8		e^-	7
PRNU		1.0			1.3		%	7

Note:

1. Full well capacity (FWC) is calculated by dividing the saturation level (DN) by the conversion factor (DN/e^-).
2. Non-linearity error is calculated in range between 5%-95% of the saturation level.
3. Maximum SNR is calculated by square root of the FWC (e^-), the unit of dB is 20 x log (SNR).
4. Dynamic range is the ratio of FWC (e^-) to Temporal dark noise (e^-).
5. The measurement result equals to QE x FF (fill factor).

6. Dark current is measured at -30ºC, the die temperature for this measurement is around -30ºC obtained by calibration of the die temperature sensor.

7. DSNU and PRNU results are both measured with full scale image without defect rows or columns.

8. All measurement methods are based on the EMVA Standard 1288 (Release 4.0) if no special noted.

9. All of the above key specifications are measured at die temperature of -30ºC, excepr QE.

Temporal Dark Noise Distribution

The curve below shows the cumulative histogram for temporal dark noise distribution with 14-bit STD mode.

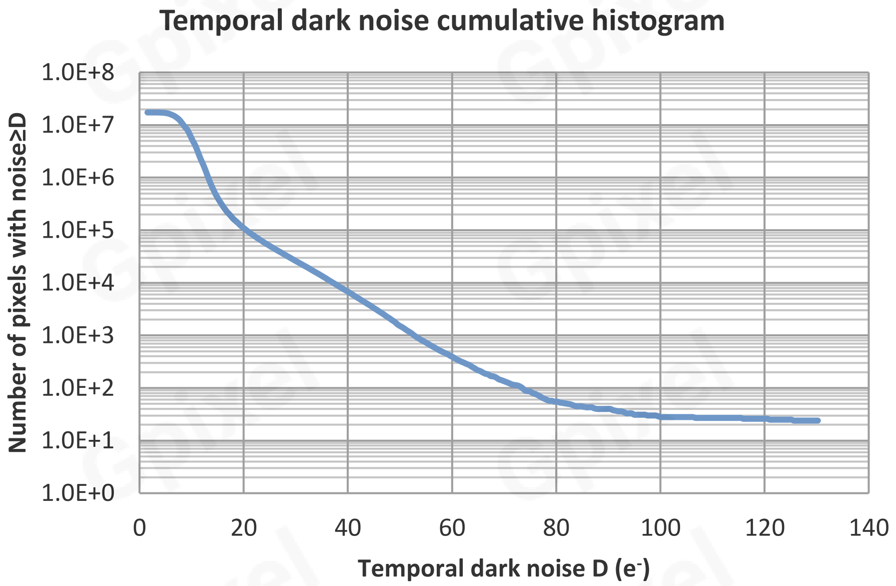


Figure 8: Temporal dark noise distribution for 14-bit STD LG

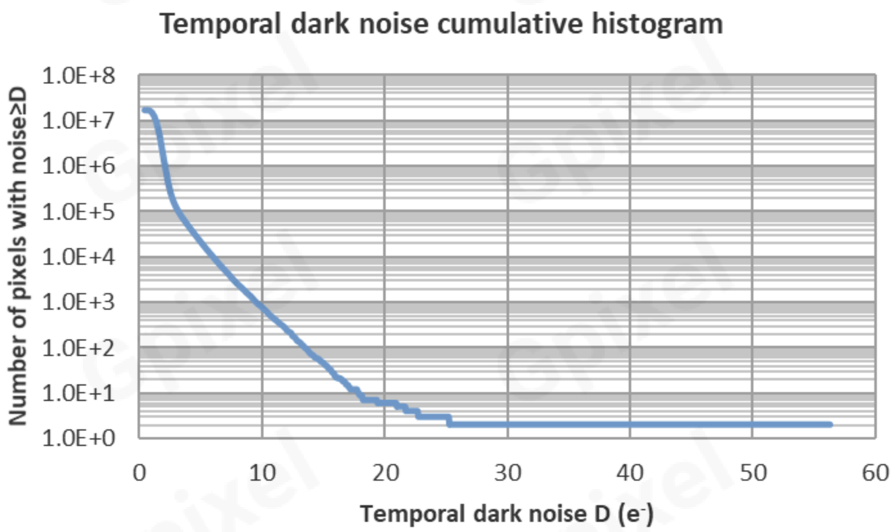


Figure 9: Temporal dark noise distribution for 14-bit STD HG

The curve below shows the cumulative histogram for temporal dark noise distribution with 12-bit HDR mode.

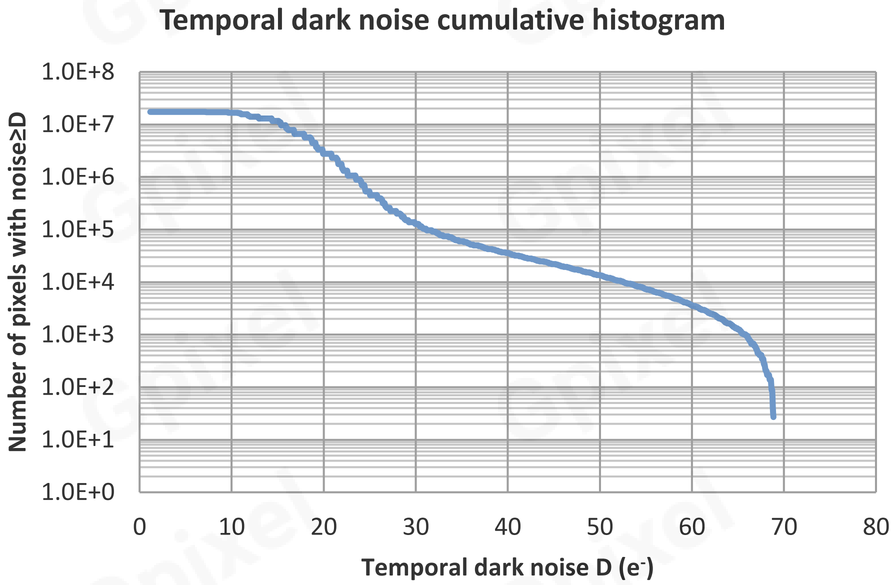


Figure 10: Temporal dark noise distribution for 12-bit HDR LG

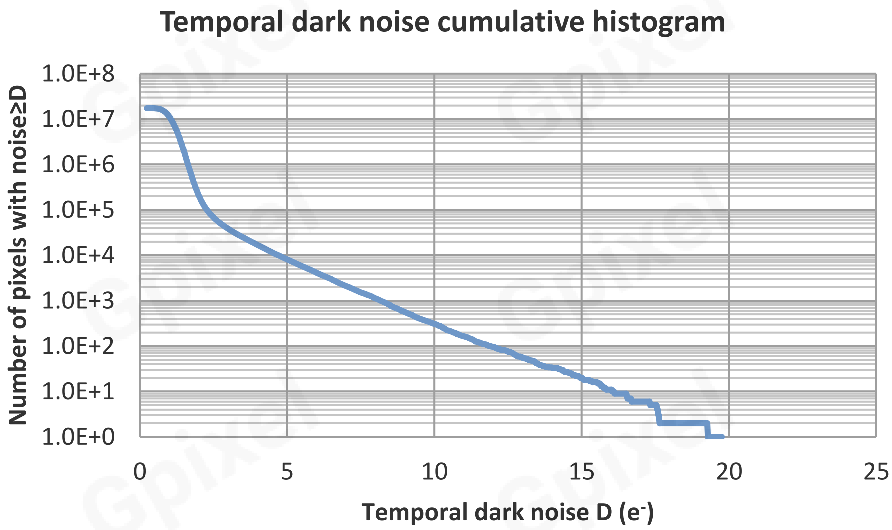


Figure 11: Temporal dark noise distribution for 12-bit HDR HG

Spectral Sensitivity Characteristics

The curve below displays the spectral response for spectrum of 200nm-1100nm for mono sensors.

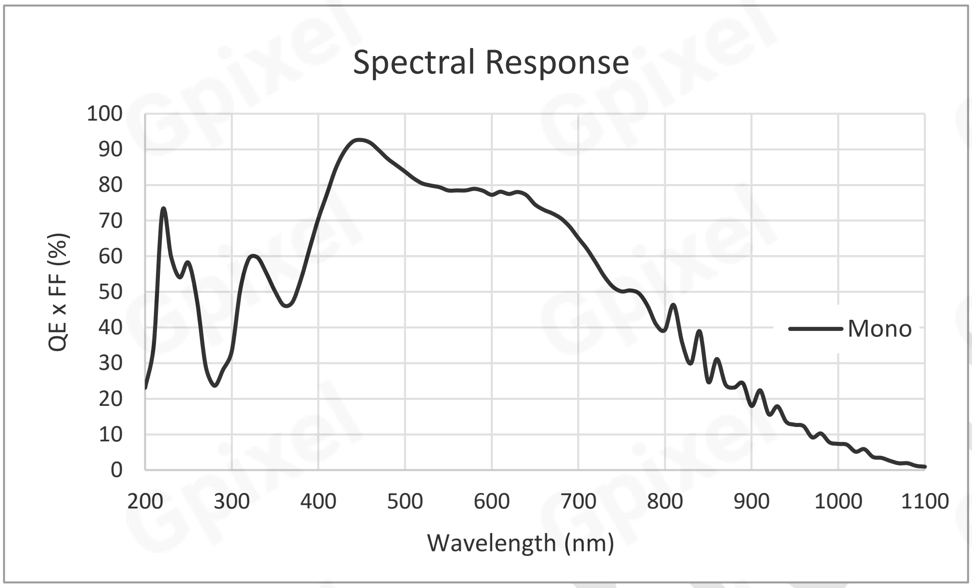


Figure 12: Spectral Sensitivity Characteristics

The table below shows more details about the QE measurement results.

Table 10: Detailed QE measurement results

Wavelength (nm)	Mono QE x FF (%)
200	23.1
250	58.2
300	33.3
350	50.1
400	70.6
450	92.6
500	83.7
550	78.5
600	77.2
650	74.5
700	65.1
750	50.1
800	39.3
850	24.7
900	18.0
950	12.7
1000	7.3
1050	3.4
1100	0.9

Dark Current with Different Die Temperature

Dark current test results with different temperature are shown below.

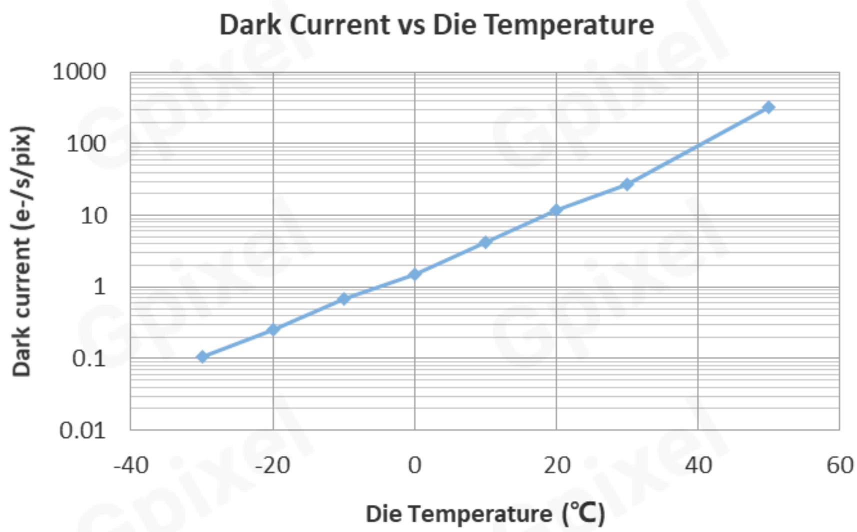


Figure 13: Dark current with different die temperature

The graph below shows the dark current distribution of the sensor tested at -30°C of die temperature. The dark current value with the most pixel counts is around 0.1 e^-/s/pix.

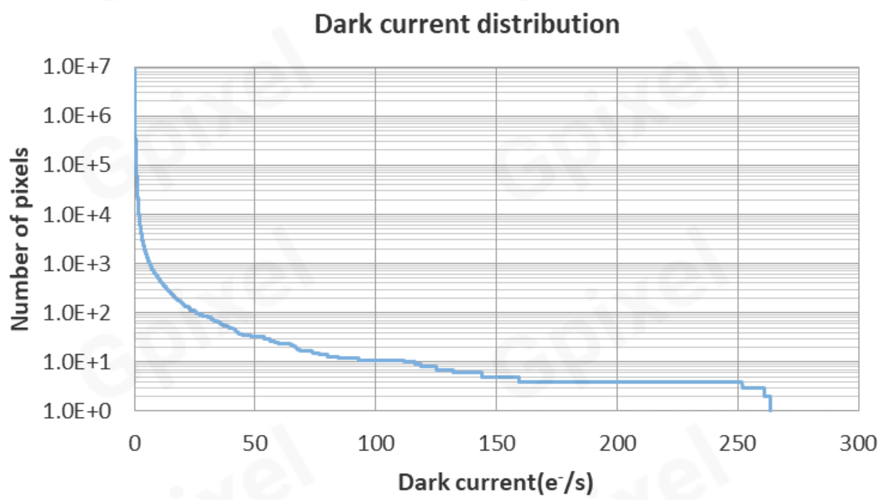


Figure 14: Dark current distribution

Angular Reponse

The sensor response depends on CRA of the incident light. To measure the angle response of the pixels, a pixel array consists of 20 pixels are selected. At each angle of the light ray, 20 grabbed images are averaged in order to reduce temporal noise influence. Then the averaged image is averaged over all its pixels. The typical angle response for the sensor can be seen in the figure below. The data includes the horizontal and vertical angles.

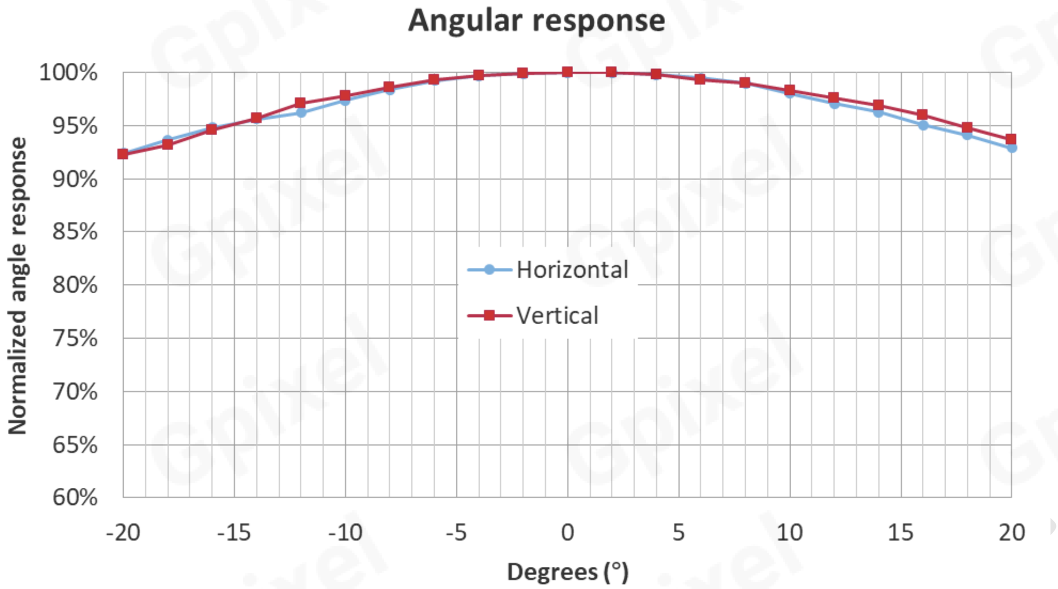


Figure 15: Angular response of the horizontal and vertical directions

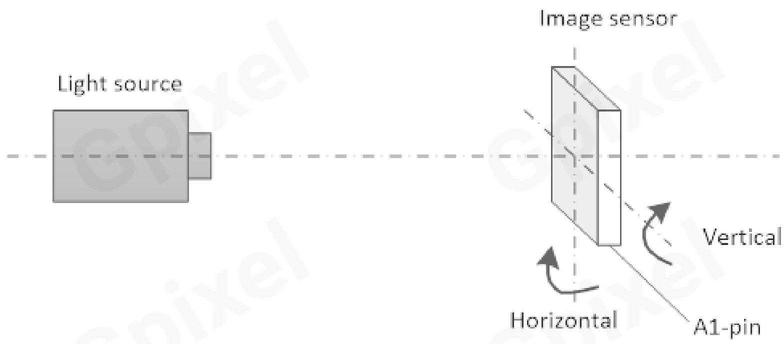


Figure 16: Horizontal and vertical definition

Register Map

Table 11: Register map

Address (hex)	Hex value		
	14-bit STD LG	14-bit STD HG	12-bit HDR
00	8A	8A	8A
01	32	32	32
02	8B	8B	BD
03	D5	C7	D5
04	33	33	33
05	8B	8B	B3
06	39	15	39
07	B3	B3	B3
08	B5	B5	B5
09	BD	BD	BD
0A	F1	F1	F1
0B	EA	EA	EA
0C	A6	A6	A6
0D	A6	A6	A6
0E	8F	8F	8F
0F	1F	21	21
10	0F	0F	0F
11	0F	0F	0F
12	8F	8F	8F
13	A7	A7	A7
14	0F	0F	0F
15	0F	0F	0F
16	0F	0F	0F
17	0D	0D	0D
18	0F	0F	0F
19	2F	2F	2F
1A	27	27	27
1B	27	27	27
1C	60	60	60
1D	3A	3A	3A
1E	7A	7A	7A
1F	00	00	00
20	69	69	01
21	25	25	02
22	50	50	50

23	00	00	A0
24	86	85	ED
25	E7	E7	DF
26	BE	BE	BE
27	7F	7F	FF
28	16	06	16
29	00	00	00
2A	00	00	00
2B	00	00	00
2C	00	00	00
2D	00	00	00
2E	00	00	00
2F	00	00	00
30	EC	EC	00
31	3D	3D	E8
32	02	02	03
33	1E	1E	3E
34	04	04	01
35	7B	7B	00
36	8F	8F	FA
37	65	65	65
38	D1	D1	D1
39	6D	6D	6C
3A	03	03	03
3B	06	06	06
3C	D3	D3	D3
3D	11	11	11
3E	A8	A8	A8
3F	07	07	07

Driving the Sensor

Sensor Setting Flow

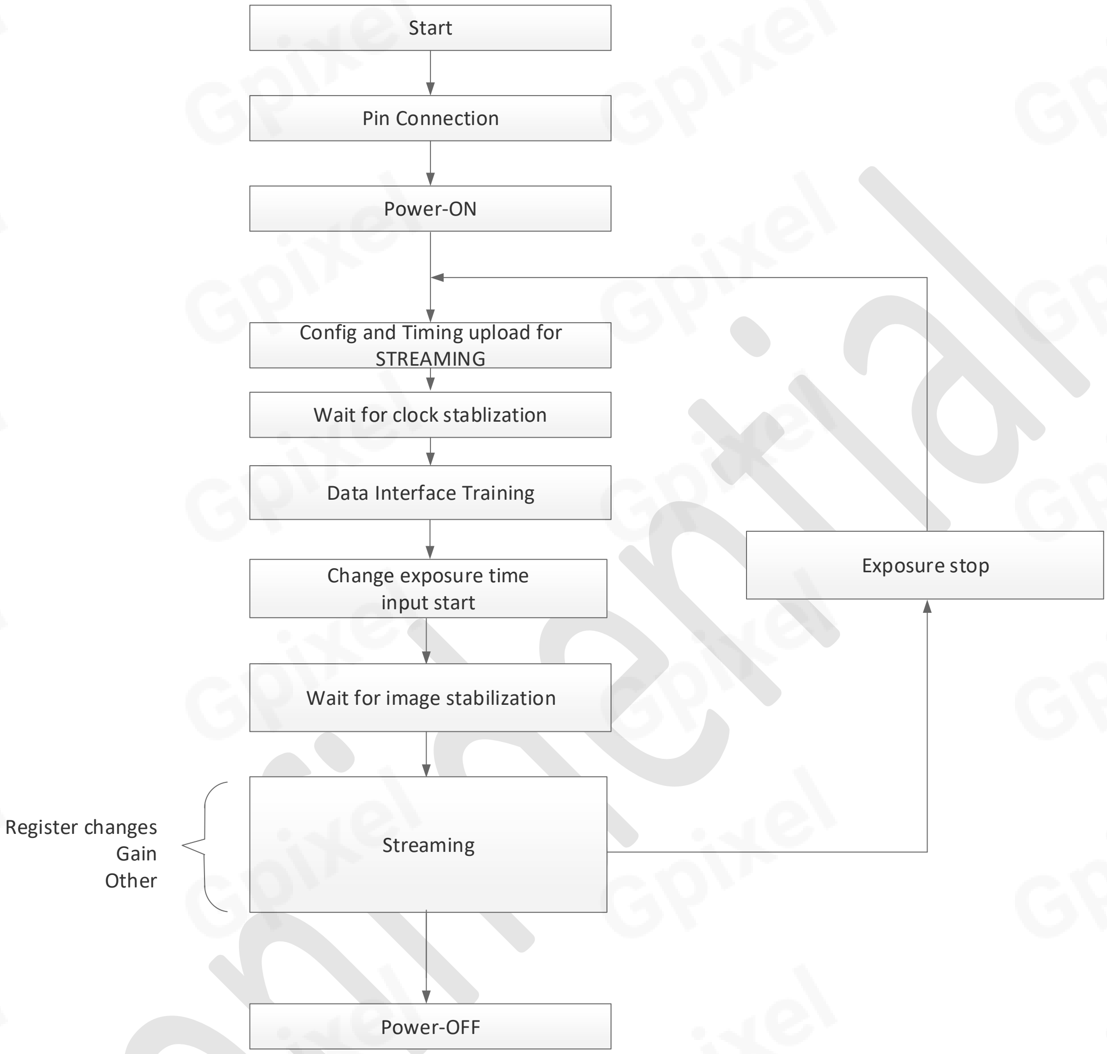


Figure 17: GSENSE1517BSI setting flow

Periphery Connections

This section shows the typical examples for hardware connections of GSENSE1517BSI. They are provided for user's reference, Gpixel does not take any responsibility for use of these circuits.

Analog Power Connections

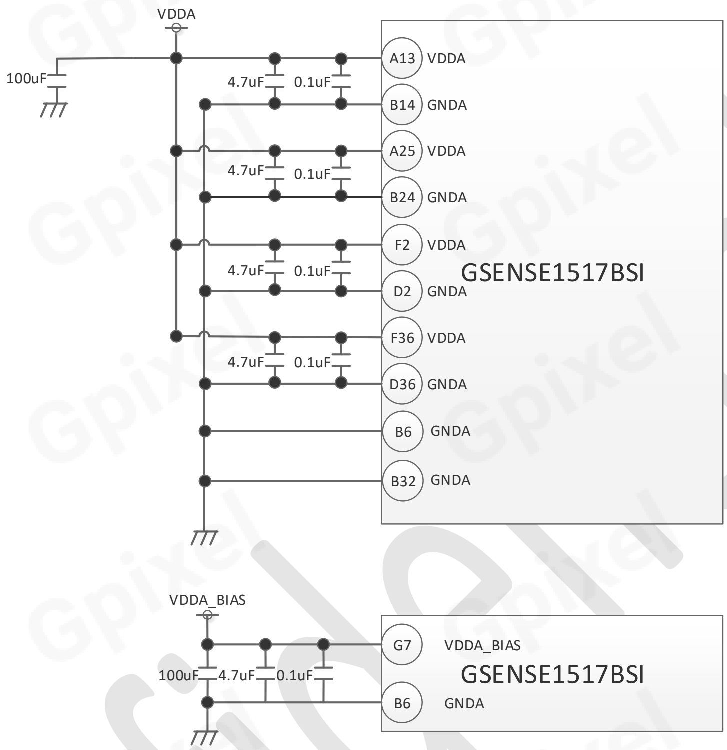


Figure 18: GSENSE1517BSI analog power/ground connections

Digital Power Connections

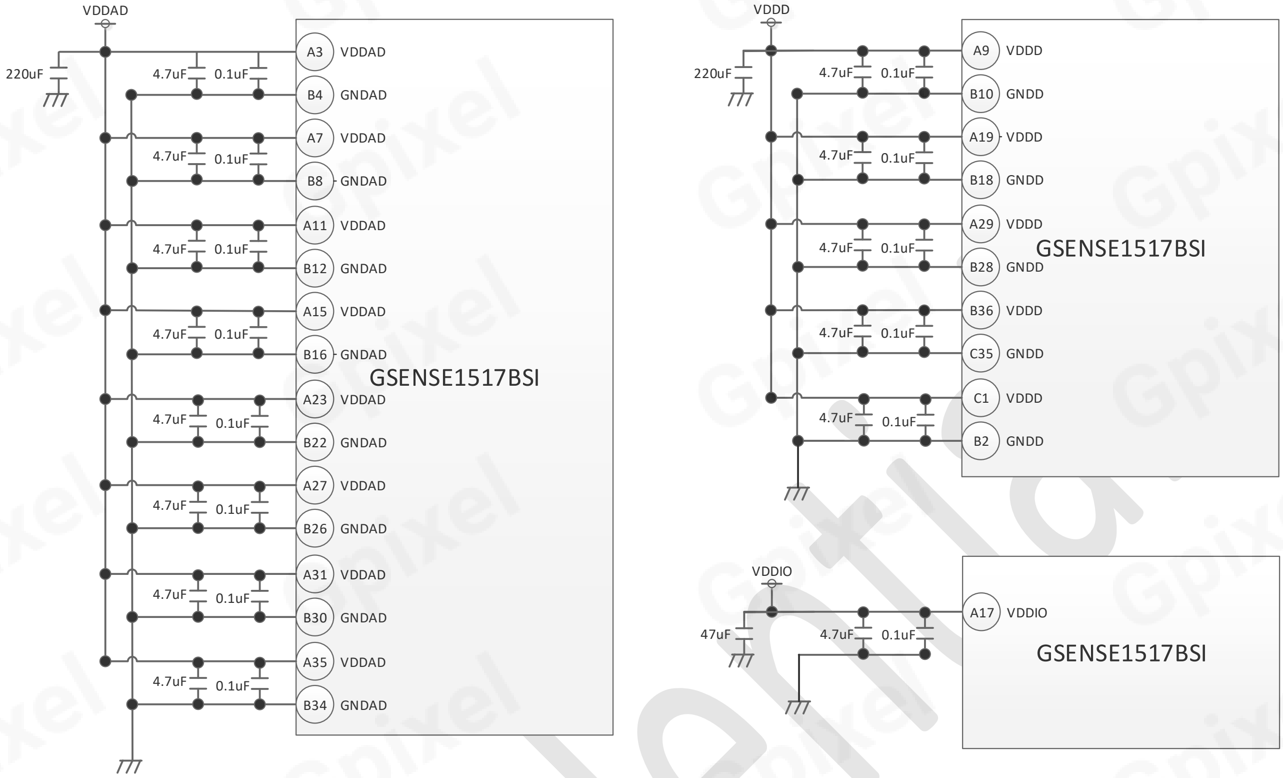


Figure 19: GSENSE1517BSI digital power/ground connections

Array Supply Connections

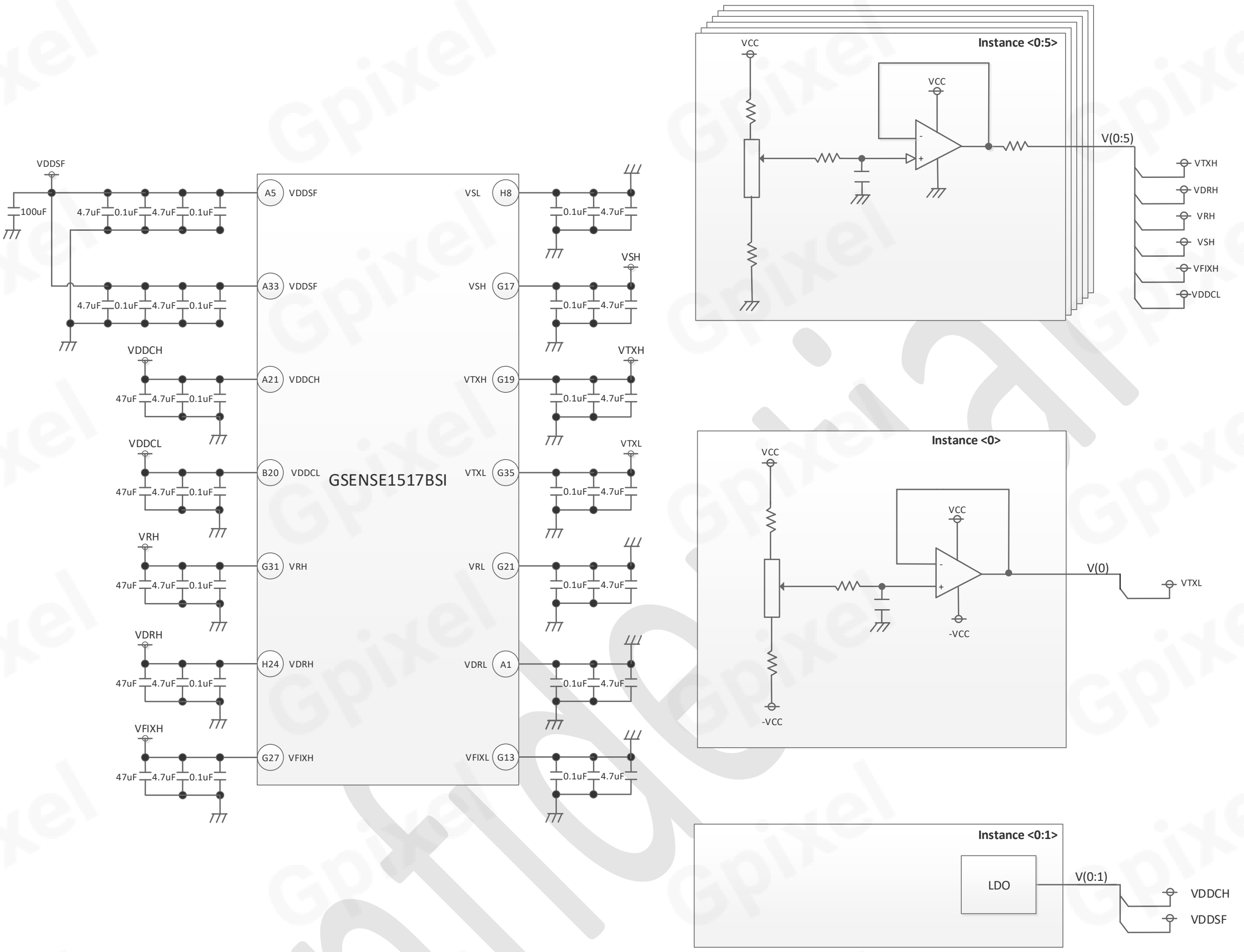


Figure 20: GSENSE1517BSI array supply connections

Note:

1. All the pixel supplies except VDDCH and VDDSF should be able to source/sink 50mA current for best performance.
2. Because the GND on Gpixel evaluation board is clean, so VRL, VDRL, VSL and VFIXL are all shorted to GND. If the GND on customer's evaluation board is not clean, please used analog buffer to power VRL, VDRL, VSL and VFIXL instead.

Bias and Reference Pin Connections

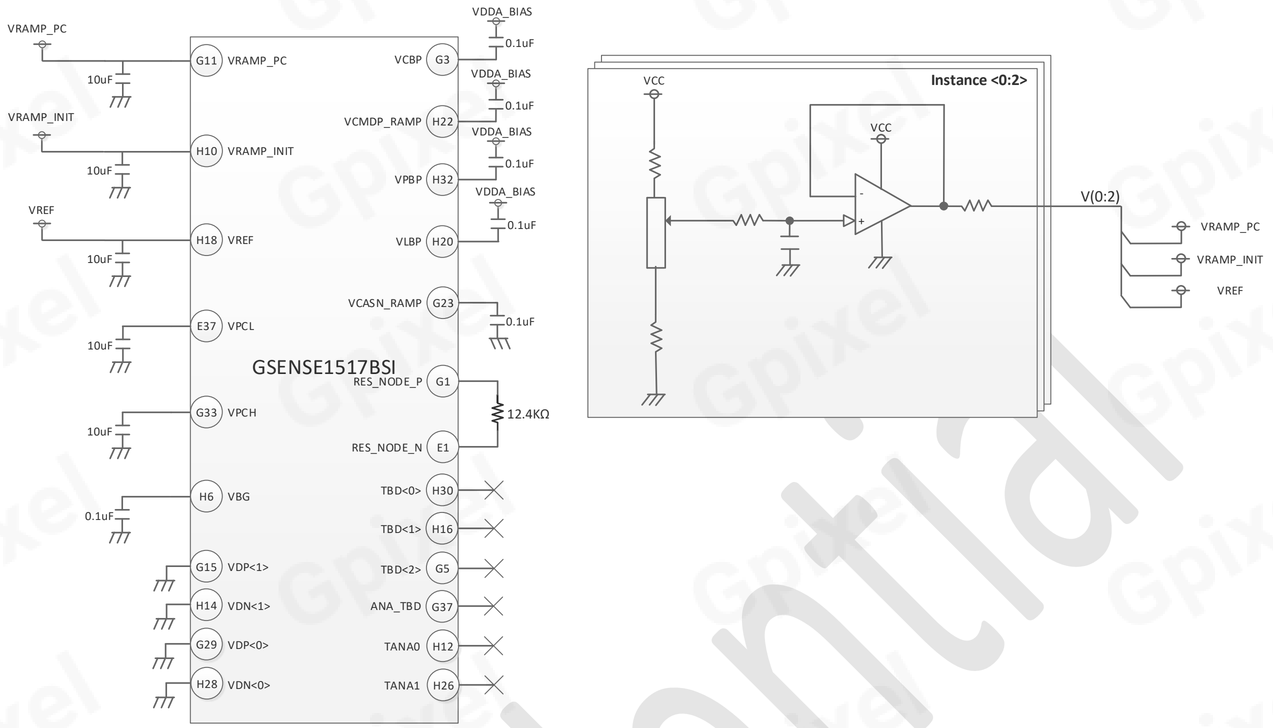


Figure 21: GSENSE1517BSI bias and reference pin connections

Digital I/O

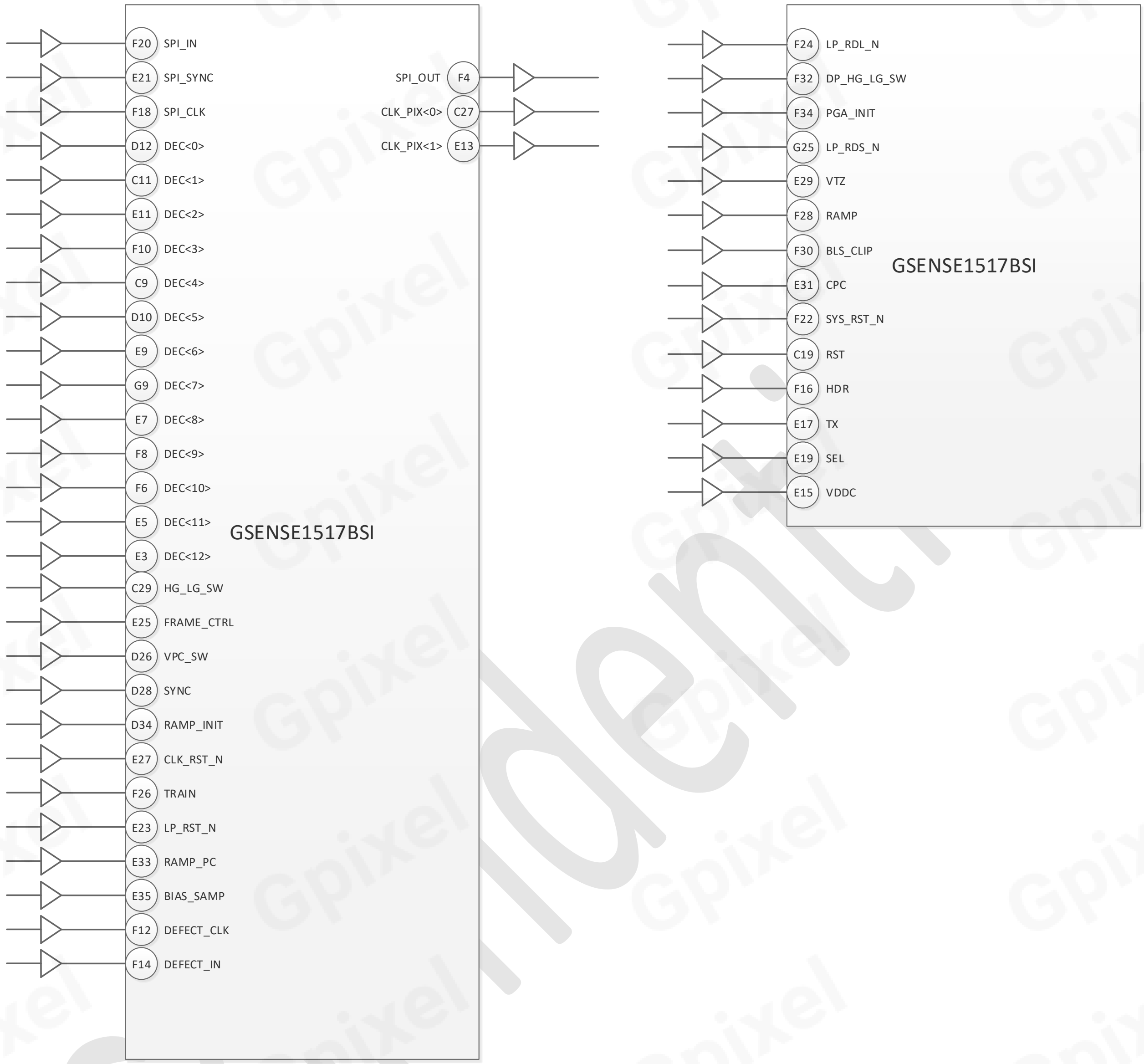


Figure 22: GSENSE1517BSI digital IO connections

LVDS Input/Outputs

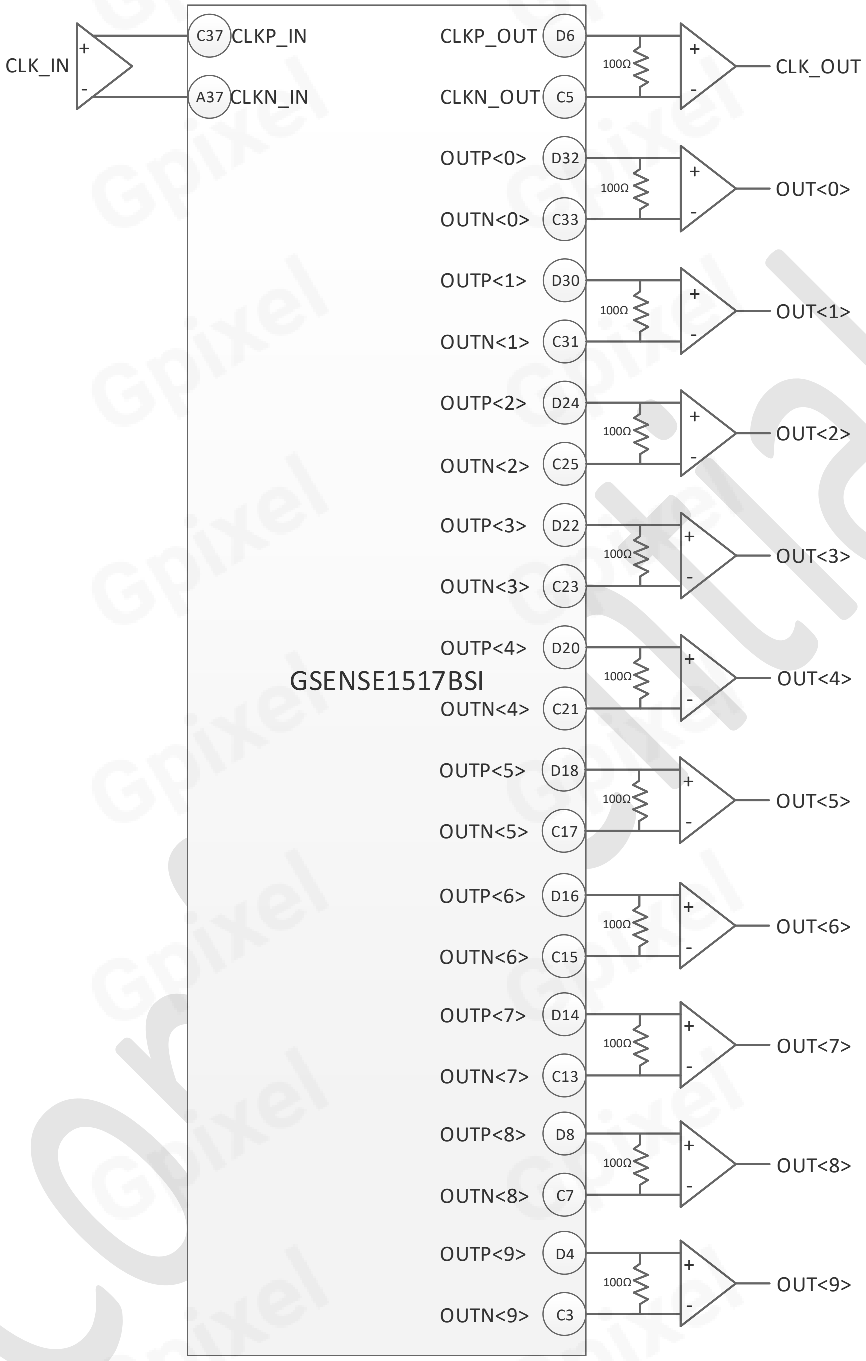


Figure 23: GSENSE1517BSI LVDS connection

Power On/Off Sequence

The power supplies should follow the power on/off sequency as illustrated in Figure 24 to avoid current peaks during power on and off. Minimum time delays should be guaranteed. CLK_SEQ in Figure 24 is the clock in FPGA to generate all the digital control signals. The frequency of this clock needs to be the same as CLK_PIX (mentioned in "CLK_PIX Calculation"), but the phase can be different. It is critical here that the CLK_RST_N needs to be kept low at least 60ms after the Supply-Group2 stabilized in order to successfully lock the phase relationship between CLK_SEQ and CLK_PIX.

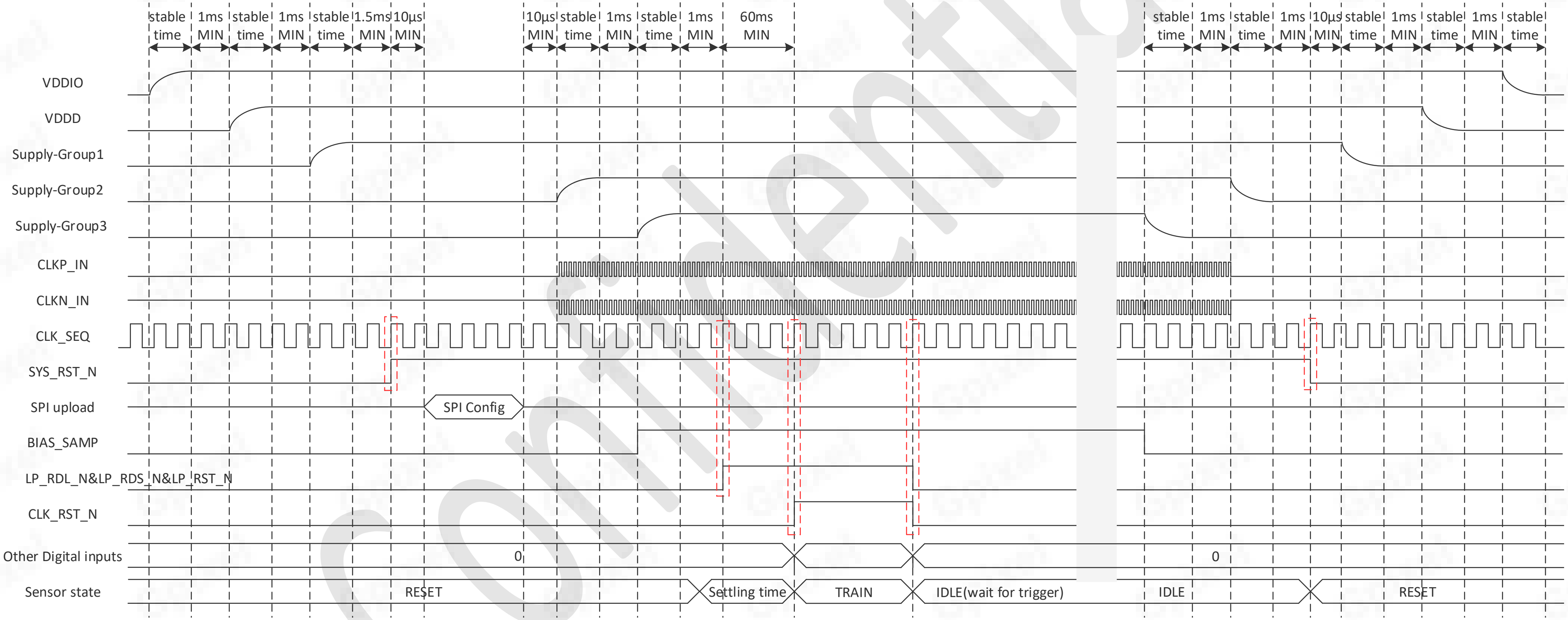


Figure 24: Power-on and power-off sequence

Supplies and references are separated in two groups which are supply1, supply2 and supply3 during power on/off, as listed in Table 12..

Table 12: Supply and reference group description during power-on/off sequence

Group	Supply1	Supply2	Supply3
Symbols	VDDA	VDDCH	VDDCL
	VDDAD	VRH	VRL
	VDDA_BIAS	VDRH	VDRL
		VTXH	VTXL
		VFIXH	VFIXL
		VSH	VSL
		VDDSF	
		VREF	
		VRAMP_PC	
		VRAMP_INIT	

Reset Sequence

The sensor reset sequence is shown in Figure 25. All the signals in the figure should follow the corresponding minimal time delays for correct reset operation. All programming registers will be reset to their default value when SYS_RST_N is set to '0'. It is necessary to reconfigure the registers before image capture. If different CLK_PIX frequency is required while the sensor running, the sensor reset sequence must be executed. Please reset the sensor when it is in IDLE state.

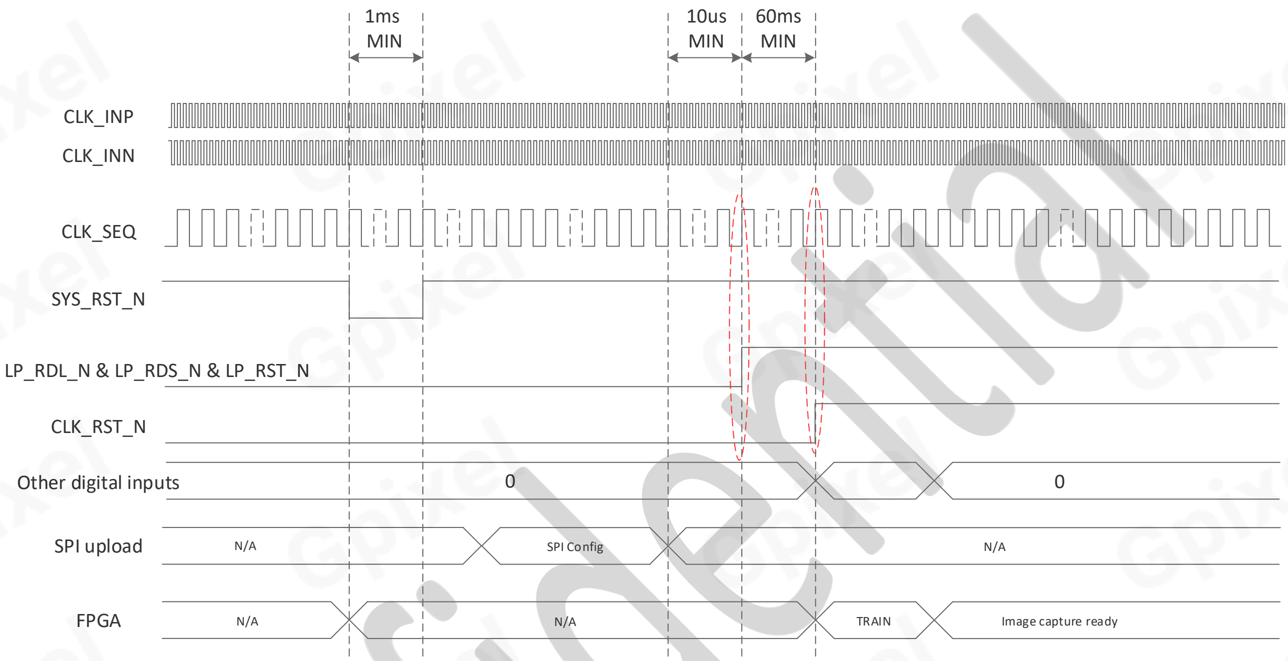


Figure 25: Sensor reset sequence

CLK_PIX Calculation

CLK_PIX is the on-chip pixel clock, which is used to calculate the exposure time and line time. CLK_PIX's frequency (f_{CLK_PIX}) is determined by the frequency of LVDS receiver input clock (f_{CLK_INP}), the resolution of ADC and the register, as below:

$$f_{CLK\_PIX} = f_{CLK\_INP}/ADC\_Depth/2^{REG\_CLKH\_HALF\_EN}$$

Where output ADC_Depth can be 12 or 14 depending on sensor operation. Please refer to for Table 11 for REG_CLKH_HALF_EN.

CLK_PIX<0>(Pin:C27) and CLK_PIX<1>(Pin:E13) are two independent output pins to output CLK_PIX. It can be disabled through SPI register setting. It is recommended to enable these two pins to see if CLK_PIX is correct during camera debug phase.

Table 13: Register settings for CLK_PIX

Address (H)	Bit	Register Name	Descritption
3D	5	REG_CLKH_HALF_EN	
1E	7	REG_CLK_PIX1_SET<4:0>	CLK_PIX<1> enable control: 0: disable 30: enable
1D	7		
1B	7		
1A	7		
19	7		
18	7	REG_CLK_PIX0_SET<4:0>	CLK_PIX<0> enable control: 0: disable 30: enable
17	7		
16	7		
15	7		
14	7		

Register Communication Timing

GSENSE1517BSI contains in total 512 on-chip registers. These registers are divided into 64 address, each consists of a 8-bit register. The register banks can be accessed with a 15-bit Address. After the power-on or reset sequence, the default values for all registers are '0'. These registers can be programmed according to the Register Map or read via a serial-to-parallel interface (SPI). The maximum operation frequency of SPI_CLK is 1MHz.

The SPI write timing is shown in Figure 26. A 24-bit stream should be put on SPI_IN followed by a SPI_SYNC to write the data into the register bank. The data stream should be synchronized with SPI_CLK as shown in the figure. Details of the 24-bit data stream is listed below:

a) One control bit: the first bit to be sent, indicating whether the operation is write("1") or read("0").

b) 15 address bits to access the selected register bank: A<14:0>, MSB first.

c) 8 data bits: the data to be written into the selected registers, MSB first.

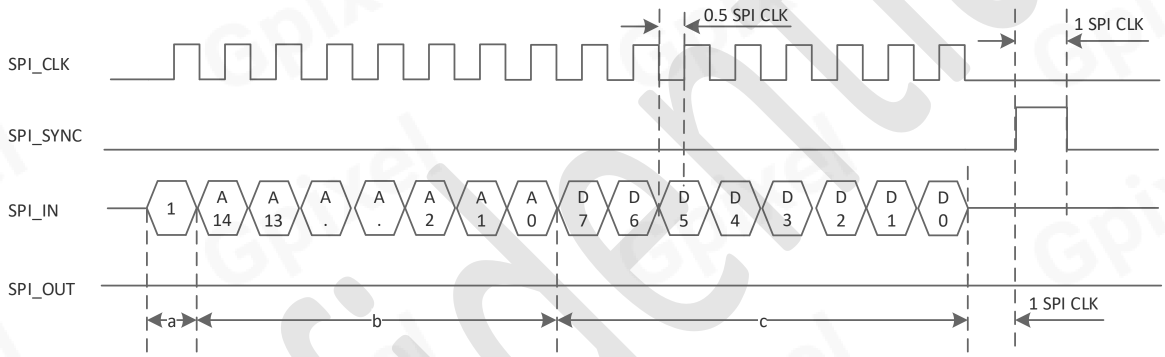


Figure 26: SPI write timing

The SPI read timing is shown in Figure 27. A 24-bit stream should be sent via the SPI_IN. The control bit should be set to '0' followed by the 15 address bit. The 8 data bit are now all set to '0'. After pulsing of SPI_SYNC, the corresponding 8-bit registers data will be read out at the rising edge of SPI_CLK with MSB first.

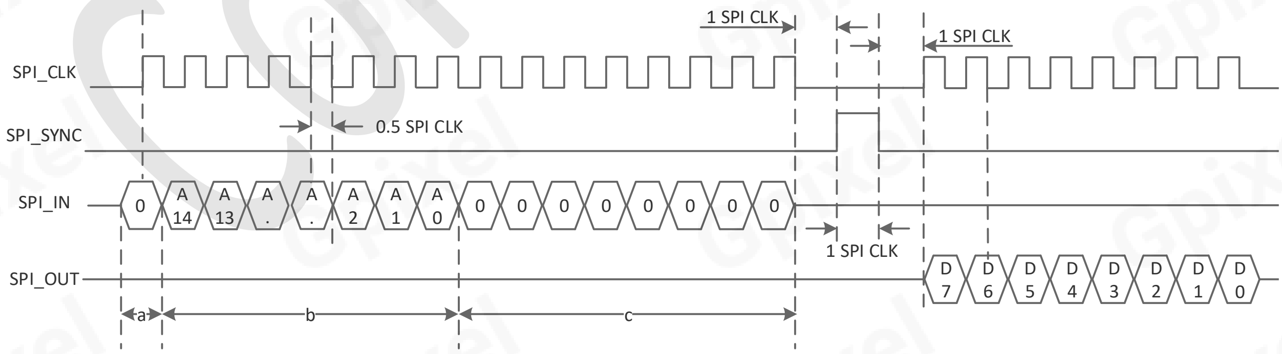


Figure 27: SPI read timing

Synchronization of Digital Control Signals

All the timing control signals shown in Table 3 should be synchronized to the rising edge of CLK_SEQ(with T_{delay} neglected) within FPGA. As described in section Figure 28, the delay between the rising edge of CLK_RST_N and any edge of any control signal should be restricted as below:

$$N \times CLK\_SEQ + a$$

Where N is an integer, a is the uncertain delay which is required that |a|<5ns at the sensor pins.

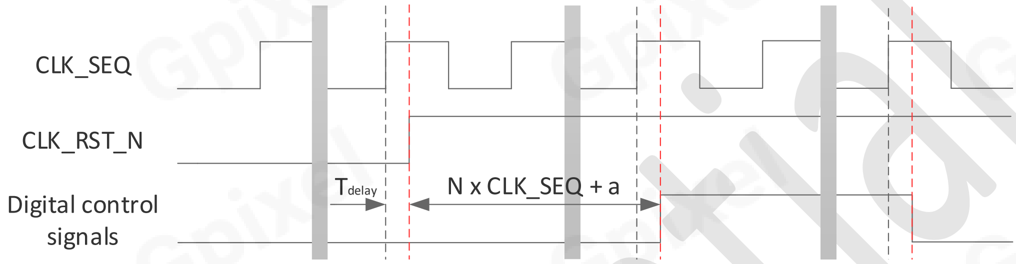


Figure 28: Synchronization of digital control signals

Pixel Row Addressing

Figure 29 shows the row accessing for GSENSE1517BSI. The whole pixel array are divided into 4 blocks, with each block containing 1048 pixel lines. Decoder inputs DEC<12:0> are used for row addressing, with each dedicated bits used for block and line address. Please refer to Table 14 for detailed description of the register. For example, if ROW<1100> needs to be addressed, DEC<12:0> should be set to B01-B00000110100 (BLOCK-LINE), with 'B' stands for binary code.

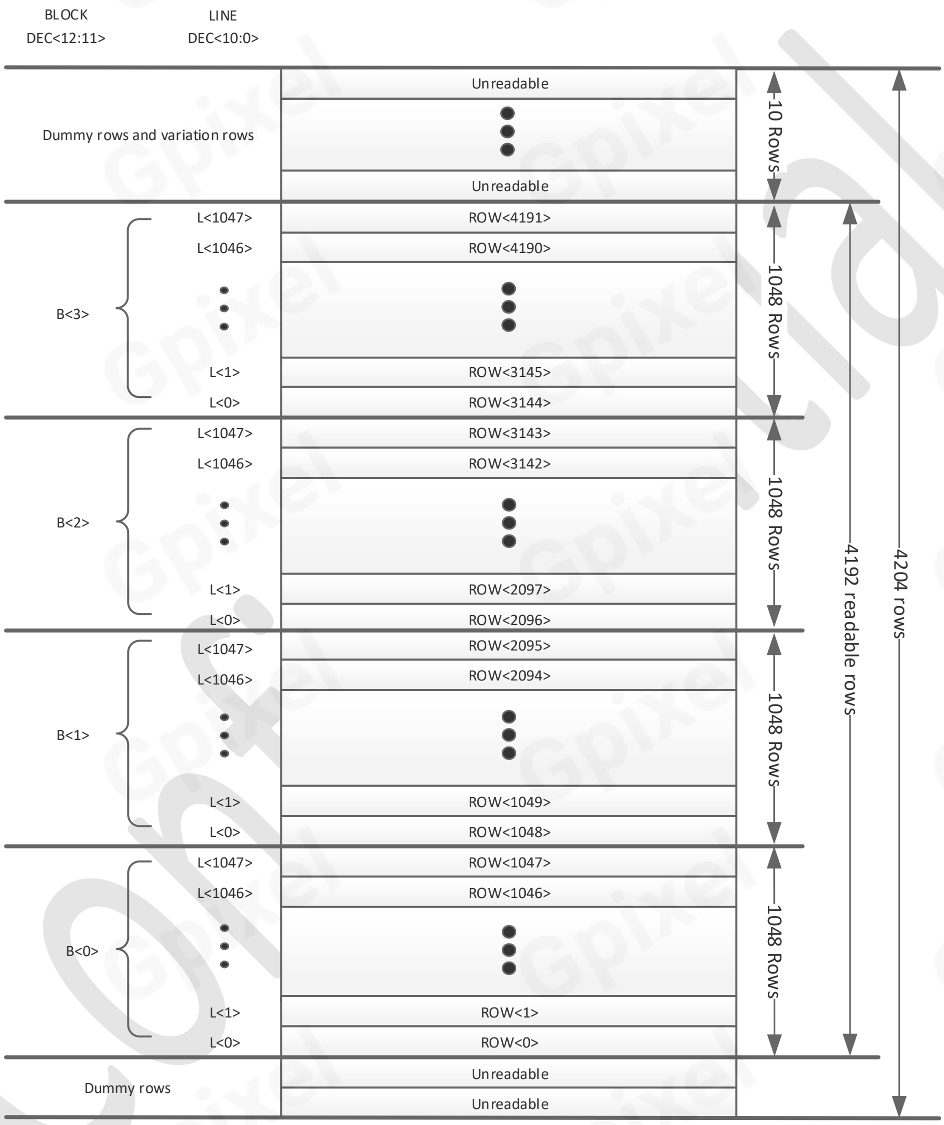


Figure 29: Row accessing for product GSENSE1517BSI

Table 14: Mapping of decoder signals and pixel row addressing

Address level	Decoder signals	Comment
Block	DEC<12:11>	Total 4 Blocks
Line	DEC<10:0>	1048 lines for block<3:0>

Operating Pixel Array

In this section, the term “line-time” is used for describing sensor’s pixel line operation. One line-time ($T_{line\text{-}time}$) is equal to a certain number of CLK_SEQs cycles based on sensor operation.

For simple description, we use a virtual address V_Addr in decoder description for array operation. The mapping of V_Addr and physical rows for different working modes is shown in Table 15 .

Table 15: Mapping of V_Addr and physical rows

V_Addr value	DEC<12:0>	14-bit STD and 12-bit HDR
0	B00-B00000000000	ROW<0>
1	B00-B00000000001	ROW<1>
⋮	⋮	⋮
1047	B00-B10000010111	ROW<1047>
1048	B01-B00000000000	ROW<1048>
1049	B01-B00000000001	ROW<1049>
⋮	⋮	⋮
2095	B01-B10000010111	ROW<2095>
2096	B10-B00000000000	ROW<2096>
2097	B10-B00000000001	ROW<2097>
⋮	⋮	⋮
3143	B10-B10000010111	ROW<3143>
3144	B11-B00000000000	ROW<3144>
3145	B11-B00000000001	ROW<3145>
⋮	⋮	⋮
4191 (MAX_{V_Addr})	B11-B10000010111	ROW<4191>

In order to drive DEC<12:0> signals correctly, users should follow as below:

1. Calculate the V_Addr value based on exposure time, physical row windowing and operation modes, refer to information below in this section.
2. Calculate the value of DEC<12:0> based on physical rows and Table 14.
3. V_Addr should be set to 0 for dummy accessing. That means DEC<12:0> should be set to B00-B00000000000.

Frame Time Settings

GSENSE1517BSI operation is always line-time ($T_{line\text{-}time}$) based, the minimum frame time $T_{frame\text{-}time}$ is calculated as:

$$T_{frame\text{-}time} = N_{V\_Addr} \times T_{line\text{-}time}$$

N_{V_Addr} is the number of valid V_Addr calculated based on the number of rows in the region of interest (ROI). In GSENSE1517BSI, the valid V_Addr corresponds to the physical row one by one, for example, if 20 physical rows are selected for windowing, N_{V_Addr} is also equal to 20.

If slower frame time is preferred, N_{dummy} needs to inserted to increase frame time, and the frame time is calculated as:

$$T_{frame\text{-}time} = (N_{V\_Addr} + N_{dummy}) \times T_{line\text{-}time}$$

Where N_{dummy} is the number of inserted dummy addresses, which is a positive integer. $T_{line\text{-}time}$ is described in section of "CLK_PIX Calculation" and "Exposure Time Settings".

The frame rate is :

$$\text{Frame rate} = 1 / T_{frame\text{-}time}$$

The above frame rate is the calculation result of multiple frames, when only one frame is preferred, the frame time is defined as time from the start of exposure to the end of the readout.

$$T_{frame\text{-}time} = (N_{V\_Addr} + N_{exp\text{-}time} + 1 + TBD) \times T_{line\text{-}time}$$

$N_{exp\text{-}time}$ is the exposure time in unit of line-time. TBD is affected by $N_{exp\text{-}time}$. When (TBD2 + $N_{exp\text{-}time}$) is greater than TBD1, TBD is equal to TBD2, otherwise, TBD is equal to TBD1. Please refer to Table 17 for TBD1 and TBD2.

Exposure Time Settings

The exposure time is configured by controlling the decoder inputs DEC<12:0>. In one line-time, the decoder has two phases: one is defined as a read phase and the other is defined as a reset phase. The read phase is always prior to the reset phase for one line-time.

Figure 30 shows the decoder phase definition.

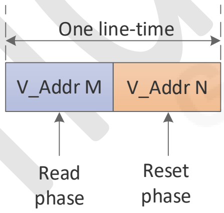


Figure 30: Decoder phase definition

The read phase means ending row exposure and reset phase means starting row exposure. The time difference between the reset phase and read phase of the same row in the same frame time defines the exposure time. The exposure time can be modified by adjusting the number of line-times ($N_{exp\text{-}time}$) between reset phase and read phase.

For single-frame applications, the exposure time needs to be equal to or larger than $1T_{line\text{-}time}$. For multi-frame applications, the exposure time can be arbitrarily set beween $1T_{line\text{-}time}$ and $T_{frame\text{-}time}$。

Figure 30 shows the simplified virtual address V_Addr operation of a single frame with invalid reset and read omitted.

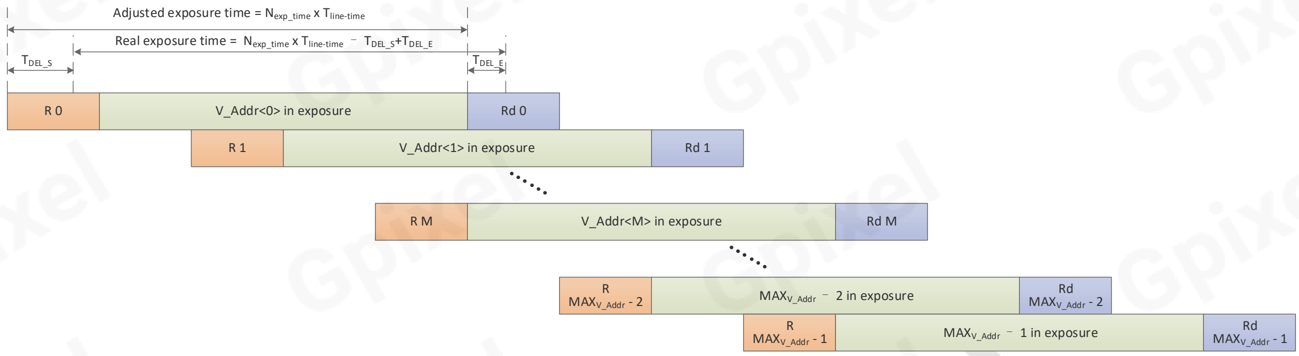


Figure 31: Simplified virtual address V_Addr operation of a single frame

The real exposure time T_{exp} is calculated as:

$$T_{exp} = N_{exp\text{-}time} \times T_{line\text{-}time} - T_{DEL\_S} + T_{DEL\_E}$$

$N_{exp\text{-}time}$ is the number of line-time, which is controlled by the decoder operation. The line time $T_{line\text{-}time}$, T_{DEL_S} and T_{DEL_E} can be calculated as

$$T_{line\text{-}time} = N_{line\text{-}time} \times T_{CLK\_SEQ}$$

$$T_{DEL\_S} = N_{DEL\_S} \times T_{CLK\_SEQ}$$

$$T_{DEL\_E} = N_{DEL\_E} \times T_{CLK\_SEQ}$$

T_{CLK_SEQ} is defined as the period of CLK_SEQ. $N_{line\text{-}time}$, N_{DEL_S} and N_{DEL_E} are listed in Table 16.

Table 16: N_{line_time} with different operation

Operation mode	12-bit HDR		14-bit STD LG	14-bit STD LG
	HG	LG		
$N_{line\text{-}time}$	2086		1788	
N_{DEL_S}	26		6	6
N_{DEL_E}	1488	840	674	678

Note：

For simple description, the exposure time in below sections has a unit of line-time cycle (with T_{DEL_S} and T_{DEL_E} neglected) if otherwise noticed.

Request Frame

Request Single Frame

Figure 32 shows the sensor virtual address V_Addr operation of a single full frame with the exposure time of three line-time. Although both read and reset phases must be present in each line-time, reset phase and read phase are shown separately in the figure to simplify the description. Read phase and reset phase within the same line-time are framed by a black dashed line.

When the frame request arrives, the reset phase is first switched from IDLE state to the start virtual address of the ROI, then incremented to the end virtual address with one virtual address per step, and finally switched back to IDLE state. The read phase requires a delay of $N_{exp\text{-}time}$ line-time before the same virtual address operation is performed. $N_{exp\text{-}time}$ is the exposure time in unit of line-time. Please note that the virtual address of reset and read phase in IDLE state must be set to Dummy address.

Figure 33 describes the virtual address V_Addr movement of a single frame with exposure time set to (N_{V_Addr} + 3) line-time.

The start virtual address (S_{V_Addr}) in Figure 32 and Figure 33 is 0, and the number of selected virtual addresses (N_{V_Addr}) is MAX_{V_Addr}.

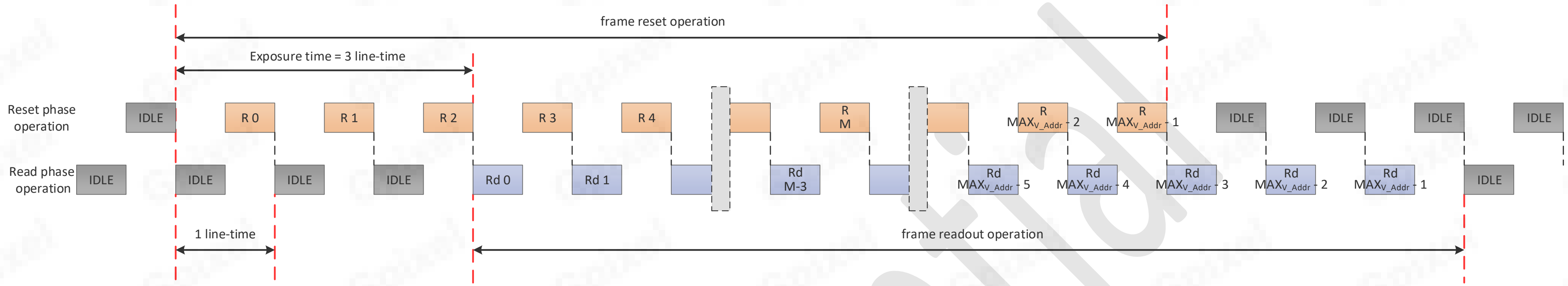


Figure 32: Virtual address V_Addr operation of single frame when exposure time is set to three line-time

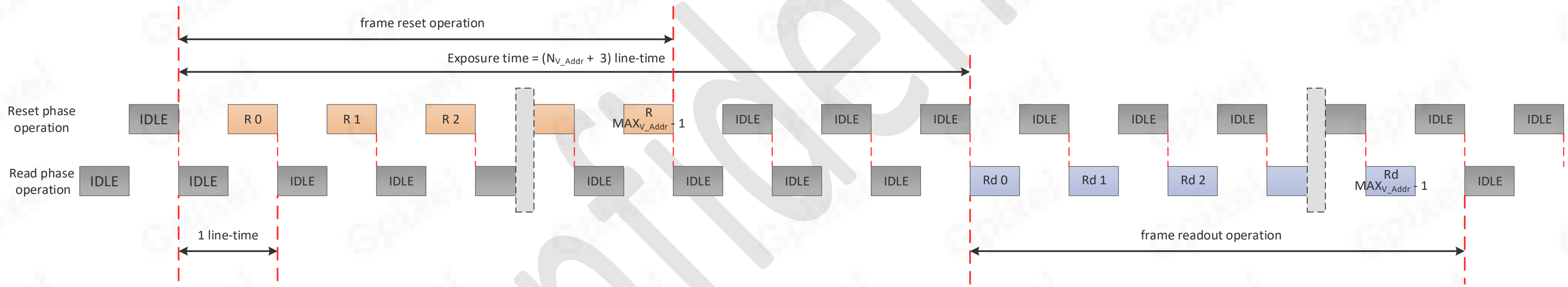


Figure 33: Virtual address movement of single frame when exposure time is (N_{V_Addr} + 3) line-time

Request multiple Frame

If more frames are required, it is possible to start next frame immediately after the previous frame ends. The virtual address movement is shown in Figure 34 with three frames required. To simplify the description, only 5 virtual addresses (S_{V_Addr} = 0, N_{V_Addr} = 5) are taken as an example.

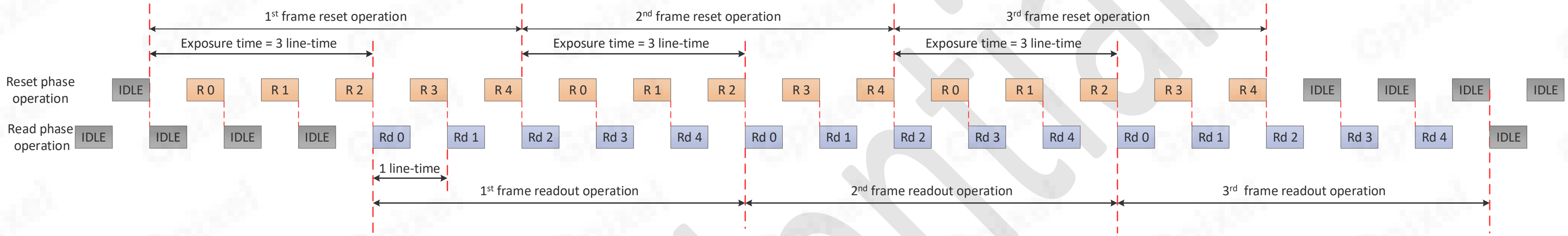


Figure 34: Virtual address movement of three frames with minimum frame time

When slower frame time is preferred, the dummy address (N_{dummy}) needs to be inserted after the valid virtual address to increase the frame time. So a full frame reset or read operation contains both valid virtual addresses and dummy addresses . As shown in Figure 35, 5 valid virtual addresses and 3 dummy addresses (S_{V_Addr} = 0, N_{V_Addr} = 5, N_{dummy} = 3) are taken as an example.

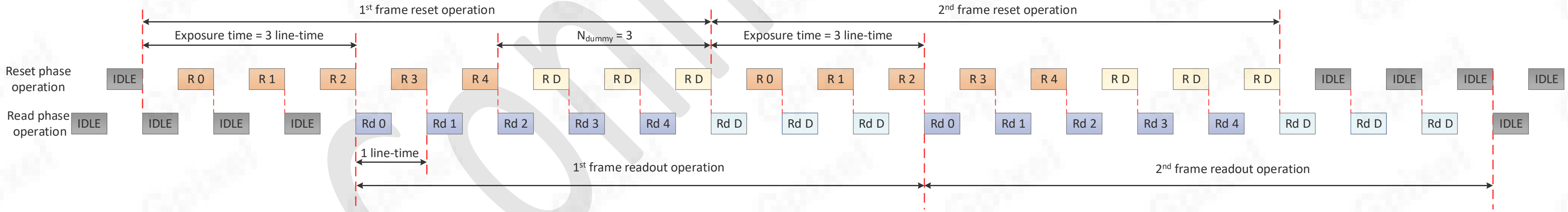


Figure 35: Virtual address movement of two frames with slower frame time

Timing of Control Signals

FRAME_CTRL and SYNC

FRAME_CTRL is the control signal of SOF and only affected by the read phase. FRAME_CTRL should be provided in the first read valid line-time or first two read valid line-time of each frame. The details of FRAME_CTRL are shown in Figure 36 and Figure 37 respectively. S_{V_Addr} is the start virtual address of the ROI, N_{V_Addr} is the number of seletcted virtual addresses, (S_{V_Addr} + N_{V_Addr} – 1) is the end virtual address.

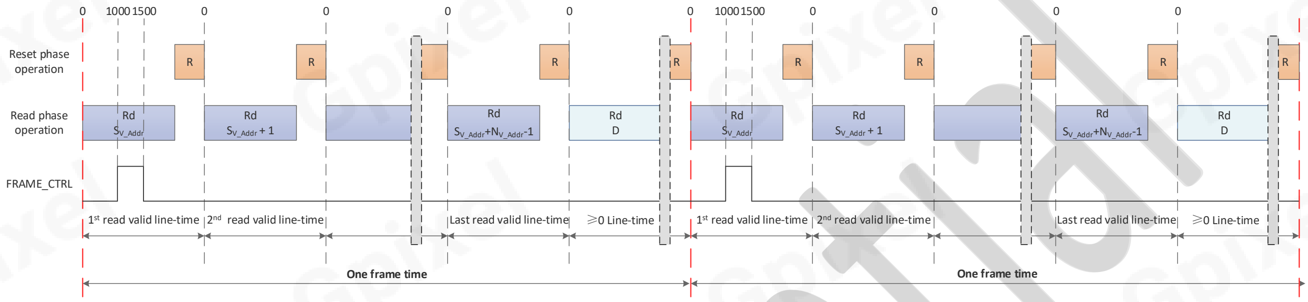


Figure 36: control timing of FRAME_CTRL in 12-bit HDR mode

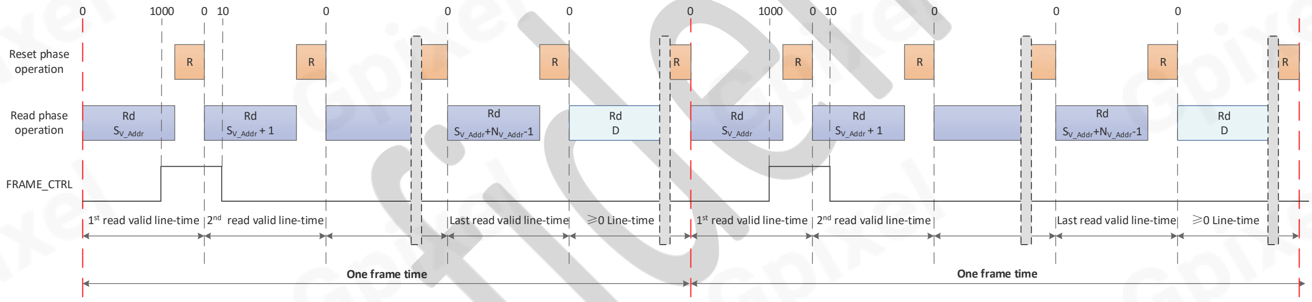


Figure 37: control timing of FRAME_CTRL in 14-bit STD mode

SYNC is the control signal used to generate SYNC Code and only affected by the read phase. As shown in Figure 38, SYNC should be provided only when read phase is valid, and the rest of the time SYNC should be 'low'. S_{V_Addr} is the start virtual address of the ROI, N_{V_Addr} is the number of seletcted virtual addresses, (S_{V_Addr} + N_{V_Addr} – 1) is the end virtual address. The periodic pulse of SYNC is shown in Figure 46, Figure 47 and Figure 48 respectively.

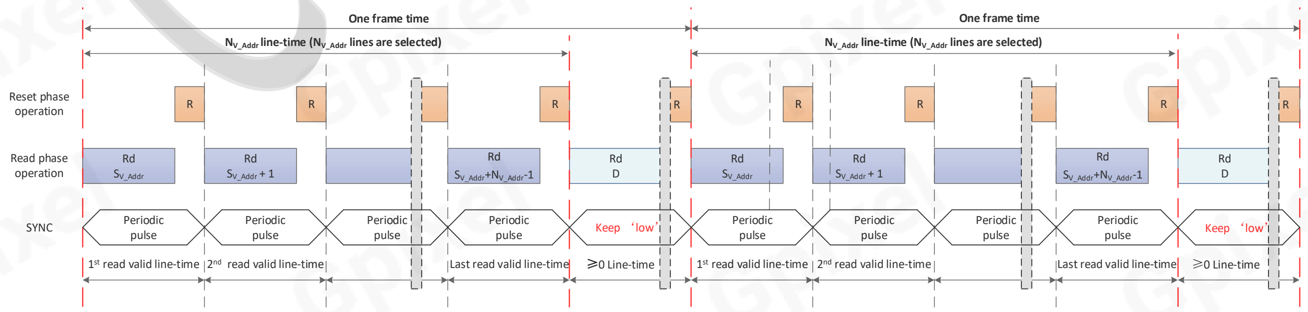


Figure 38: control timing of SYNC

LP_RDS_N and LP_RDL_N

LP_RDS_N and LP_RDL_N are control signals that are only affected by the frame time and read phase.

When single frame is requested, LP_RDS_N should be pulled up TBD0 line-time ahead of the start virtual read address (S_{V_Addr}), and pulled down one line-time later than the end virtual read address (S_{V_Addr} + N_{V_Addr} - 1). Details are shown in Figure 39.

When multiple frames are requested, LP_RDS_N is controlled by the frame time, details is shown in Figure 41 with two frames as an example:

1. If the frame time is less than (N_{V_Addr} + TBD0 + 2) x line-time, LP_RDS_N should be pulled up TBD0 line-time ahead of the first frame readout and pulled down one line-time later than the last valid read address in the last frame.
2. If the frame time is equal to or larger than (N_{V_Addr} + TBD0 + 2) x line-time, LP_RDS_N is a periodic signal with frame time as period and (N_{V_Addr} + TBD0 +1) x line-time as pulse width.

Compared with LP_RDS_N, LP_RDL_N has the same requirements as those of LP_RDS_N except that the time of pulling up in advance is TBD1 x line-time instead of TBD0 x line-time. Please refer to Figure 40 and Figure 42 for more details.

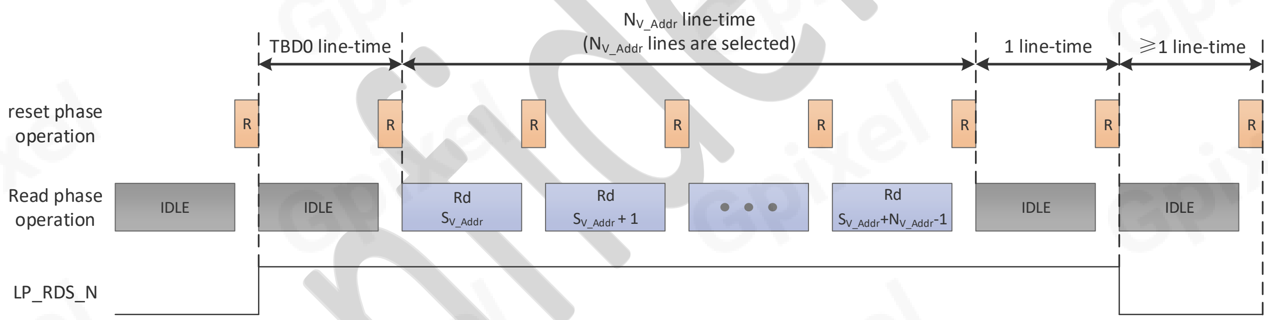


Figure 39: control timing of LP_RDS_N when a single frame is preferred

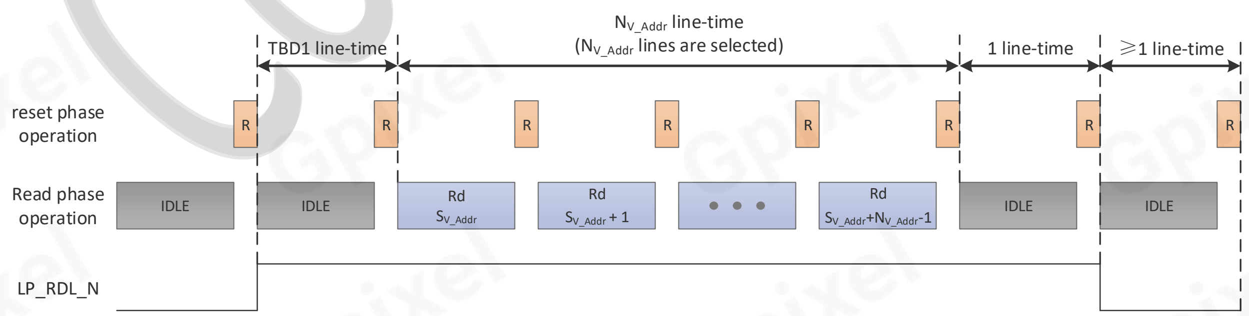
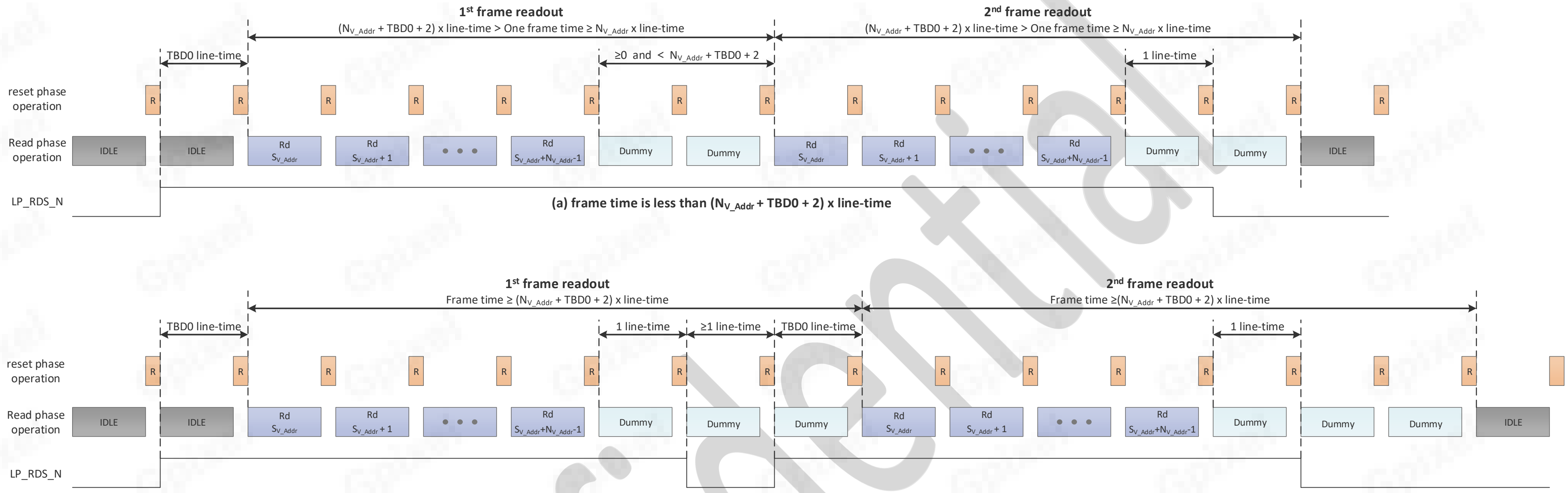


Figure 40: control timing of LP_RDL_N when a single frame is preferred



(a) frame time is less than (N_{V_Addr} + TBD0 + 2) x line-time

(b) frame time is equal to or larger than (N_{V_Addr} + TBD0 + 2) x line-time

Figure 41: control timing of LP_RDS_N when two frames are requested

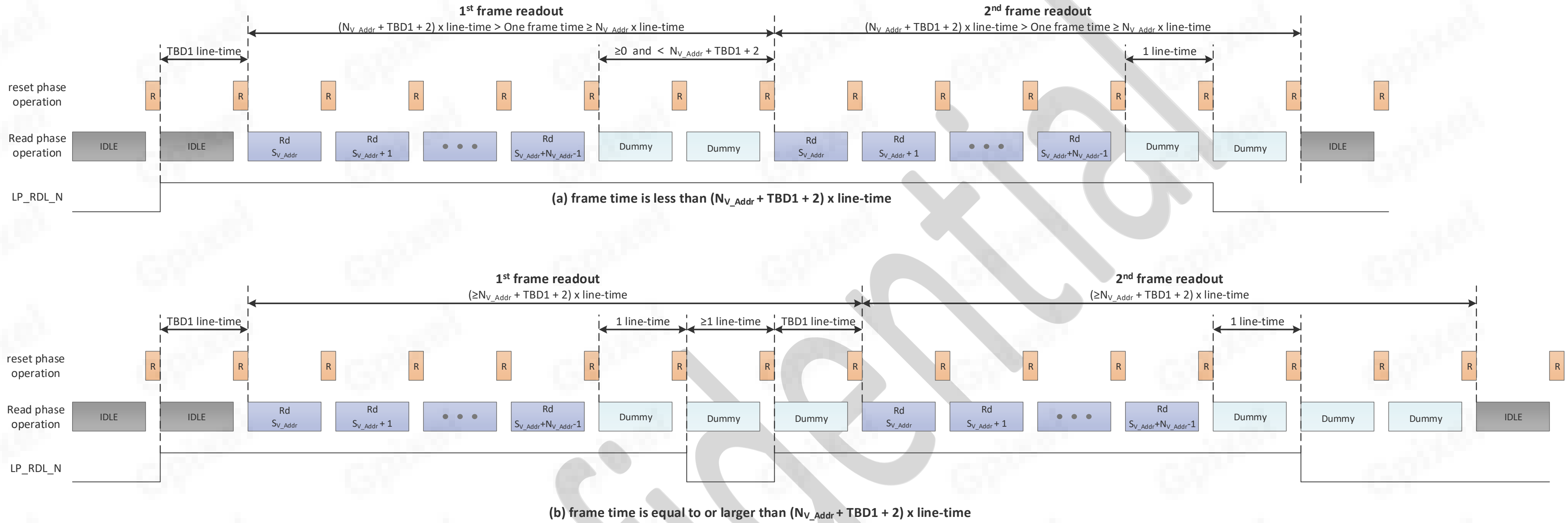


Figure 42: control timing of LP_RDL_N when two frames are requested

LP_RST_N

Unlike other control signlas, LP_RST_N are controlled by both frame time, reset phase and read phase. For simple description, the requirements for LP_RST_N during read phase and reset phase are decribed separately.

LP_RST_N_INT is used instead of LP_RST_N to describe the constraints of reset phase, details are shown in Figure 43 and Figure 44 respectively.

When single frame is requested, LP_RST_N_INT should be pulled up TBD2 line-time ahead of the start virtual reset address arrives (S_{V_Addr}), and pulled down one line-time later than the end virtual reset address ($S_{V\_Addr} + N_{V\_Addr} - 1$).

When multiple frames are requested, LP_RST_N_INT is controlled by the frame time, details is shown in Figure 44 with two frames as an example:

1. If the frame time is less than (N_{V_Addr} + TBD2 + 2) x line-time, LP_RST_N_INT should be pulled up TBD2 line-time ahead of the first frame reset and pulled down one line-time later than the last valid reset address in the last frame.
2. If the frame time is equal to or larger than (N_{V_Addr} + TBD2 + 2) x line-time, LP_RST_N_INT is a periodic signal with frame time as period and (N_{V_Addr} + TBD2 +1) x line-time as pulse width.

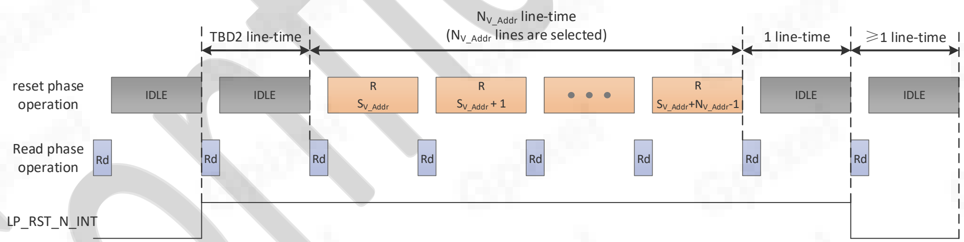


Figure 43: control timing of LP_RST_N_INT when single frame is preferred

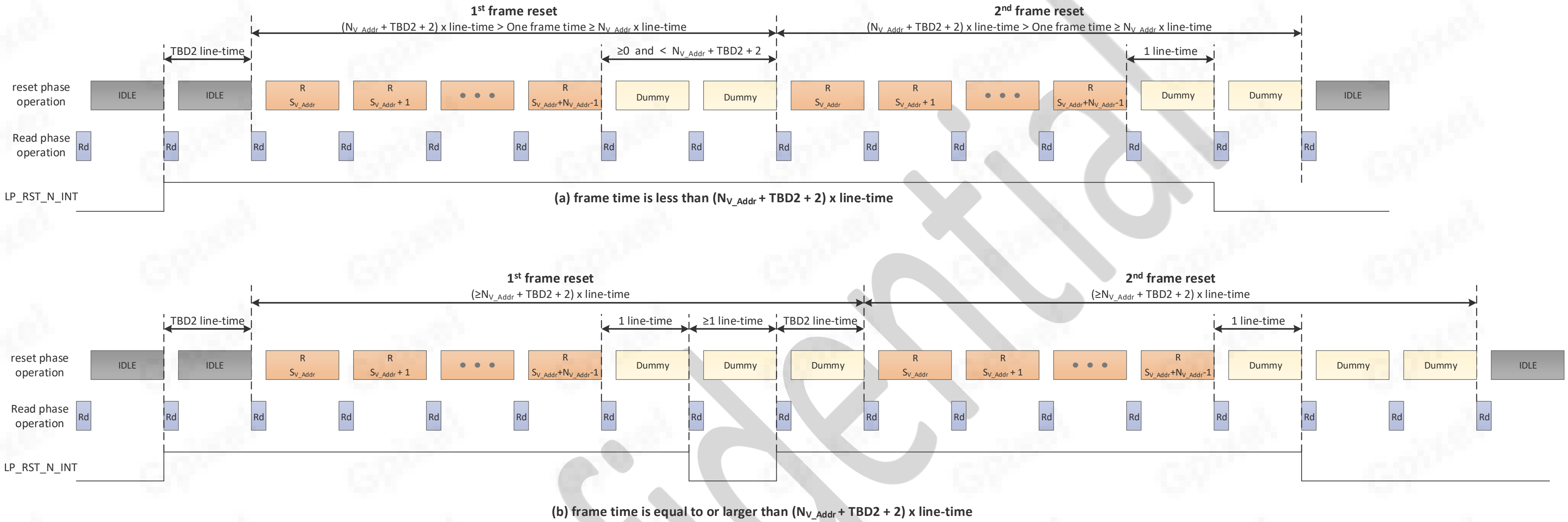


Figure 44: control timing of LP_RST_N_INT when two frames are requested

The requirements for LP_RST_N during read phase are the same as those for LP_RDL_N, so LP_RDL_N is used to represent LP_RST_N during the read phase.

The output signal after LP_RDL_N and LP_RST_N_INT perform digital logic 'or' operation is the real LP_RST_N required by GSENSE1517BSI.

Table 17: TBD0, TBD1 and TBD2 in different operation

Operation mode	12-bit HDR	14-bit STD LG	14-bit STD LG
TBD0	800	700	
TBD1	6000	5000	
TBD2	60	50	

Other Control Signals

The control timing of other control signals is divided into two states:

1. Changes with a periodic of one line-time cycles ($N_{line\text{-}time}$ x CLK_SEQ). Figure 46, Figure 47 and Figure 48 show the details with CLK_SEQ neglegted.
2. Fixed to 'high' or 'low'.

RST, VDDC, HDR, TX, SEL, CLK_RST_N all need to be pulled '0' when both LP_RDS_N and LP_RST_N are set to '0', otherwise they should be provided in accordance with periodic signals.

The other signals not described above should be provided as shown in Figure 45. These signals are all costrained by LP_RDS_N. Periodic signals need to be provided after LP_RST_N is pulled up by TBD0 line-time, and when LP_RST_N is pulled down, these signals are all pulled to a fixed level.

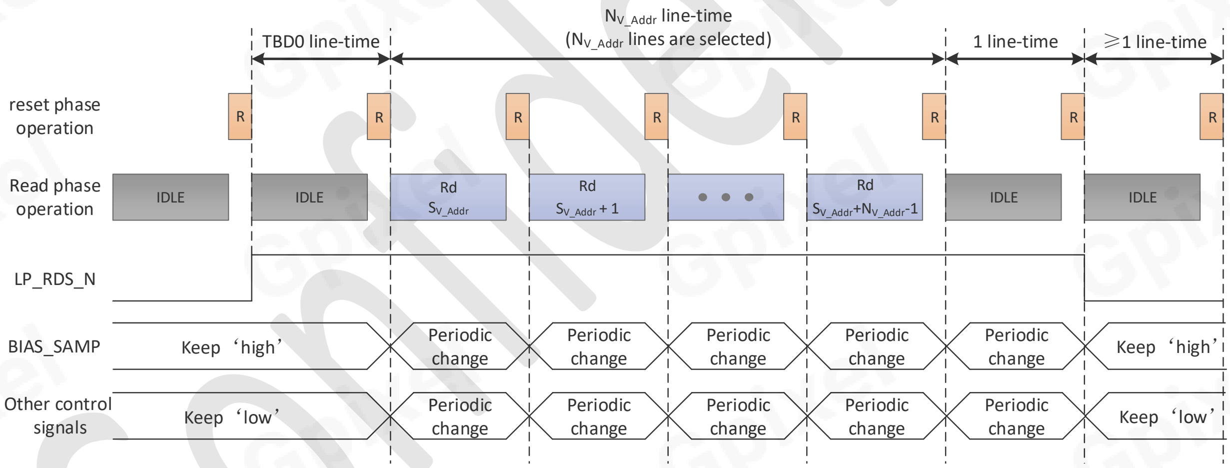


Figure 45: control timing of other control signals

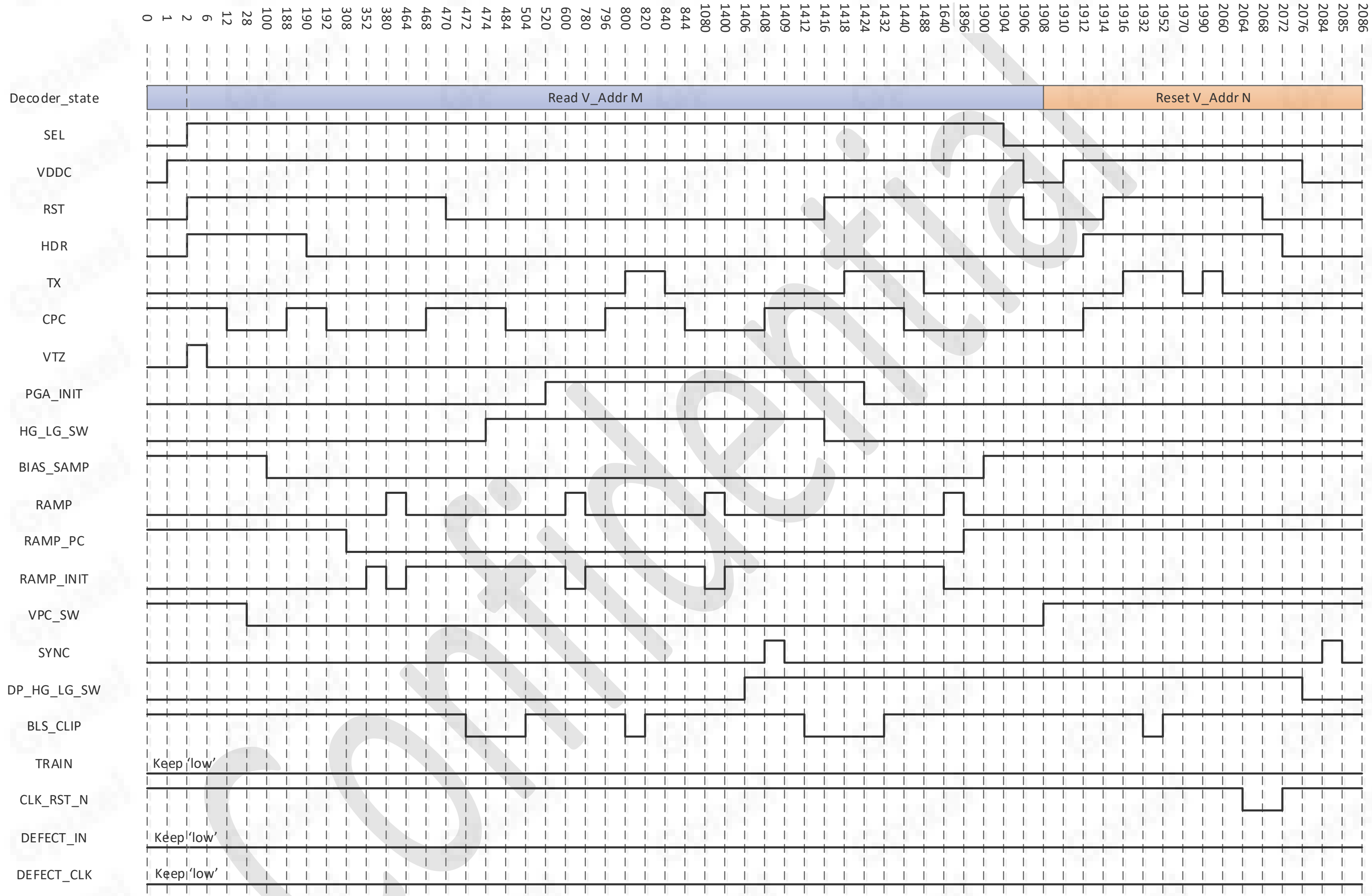


Figure 46: control timing of 12-bit HDR mode

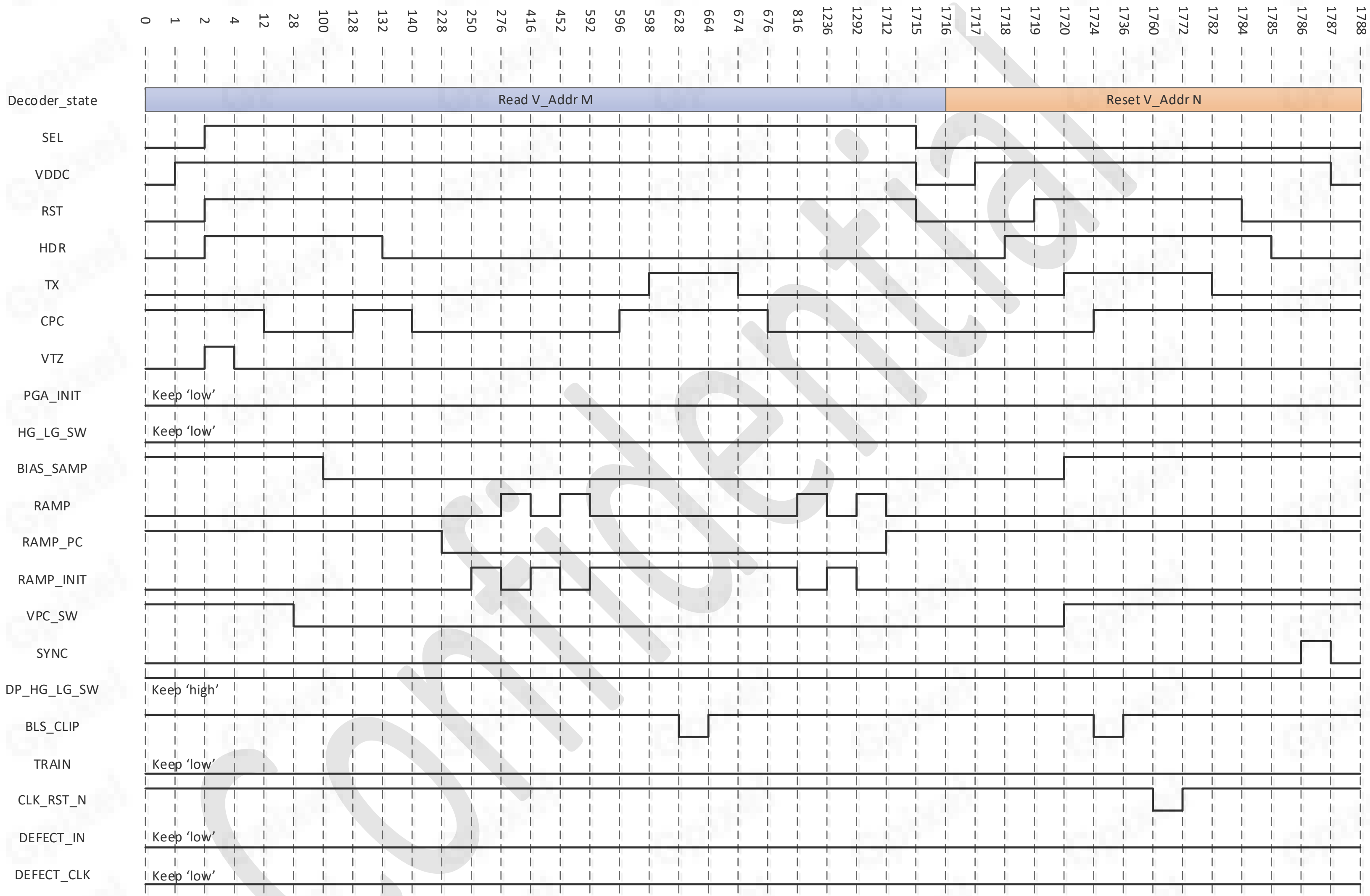


Figure 47: control timing of 14-bit STD LG mode

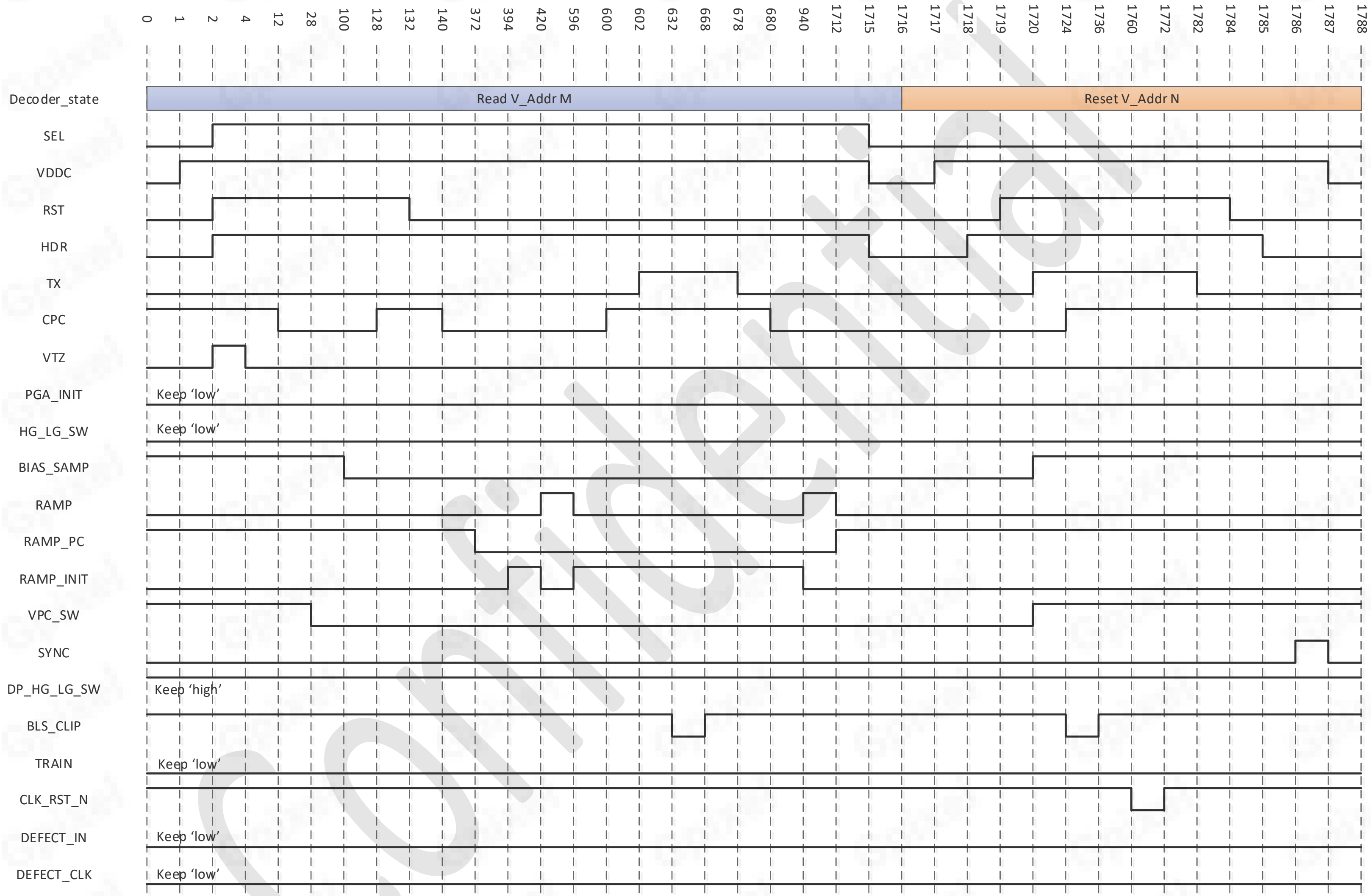


Figure 48: control timing of 14-bit STD HG mode

Reading Out The Sensor

LVDS Output

GSENSE1517BSI uses LVDS outputs for image data read out. Besides 10 LVDS data pair (DP) channels, GSENSE1517BSI has one channel for LVDS clock output, which can be used to sample the image data. This LVDS clock is a Double Data Rate (DDR) clock, with its frequency equal to half of the output data rate, for example, when output data rate is 420Mbps, the LVDS output clock is 210MHz. The illustration of LVDS output clock and LVDS data can be found in Figure 7. The DDR clock is synchronous to the 10 LVDS DP channels with minimum skew, and can be used at the receiving end for data sampling.

Please note that the DDR clock will be disabled when 'LP_RDS_N' is pulled to ground

LVDS Training

To synchronize the LVDS outputs of the GSENSE1517BSI, a known training pattern(TP) can be used as a reference on the output LVDS DPs. This reference pattern can be set by the user and used to "train" each LVDS receiver channel individually in the system. Such LVDS training is needed to avoid LVDS data misalignment due to the mismatch in the LVDS output channel design (both on chip and in electronic system).

Constantly pull 'TRAIN' high when GSENSE1517BSI starts bit correction and word correction, then all DPs will output training pattern (Programmed through SPI register REG_TRAIN_DATA<15:0> (Address<38:37>)). Figure 49 shows the details of LVDS training on one LVDS channel, T_{dealy_x} in the figure represents the delay time of LVDS channel x.

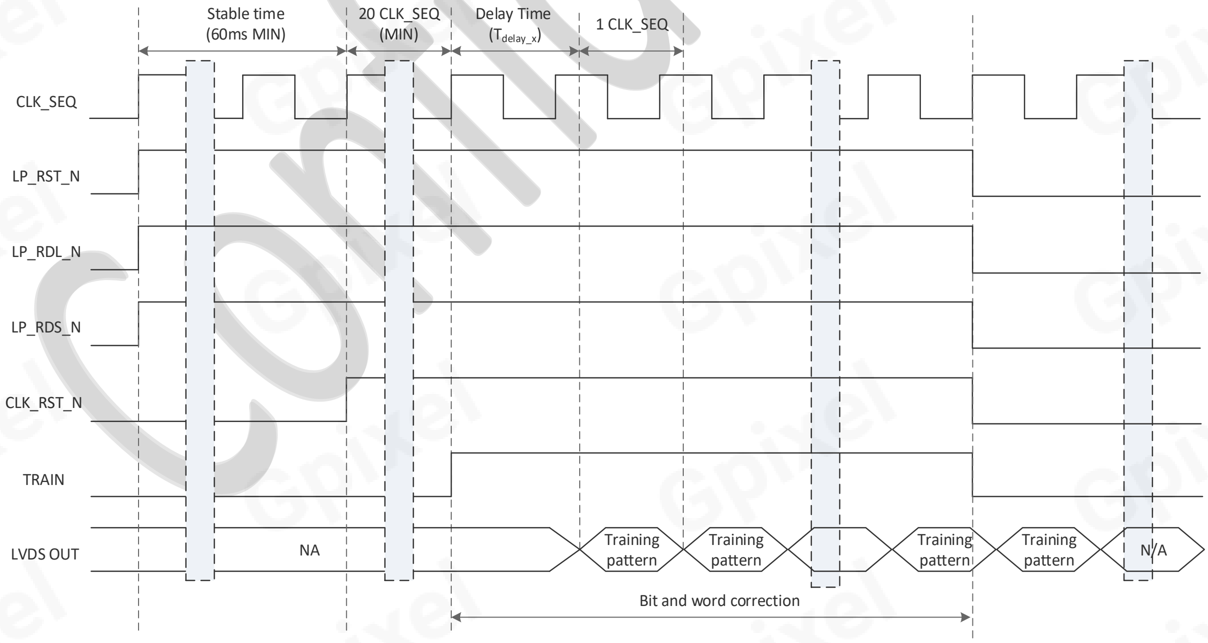


Figure 49: LVDS training on one LVDS channel

LVDS Channel Multiplexing

LVDS channnel multiplexing is supported as illustrated in Figure 50. They can be enabled through SPI register setting REG_MUX_EN<2:0>. All the un-used output channels can be disabled through SPI register setting to save power. The default setting for channel multiplexing with different operation is listed in Table 18.

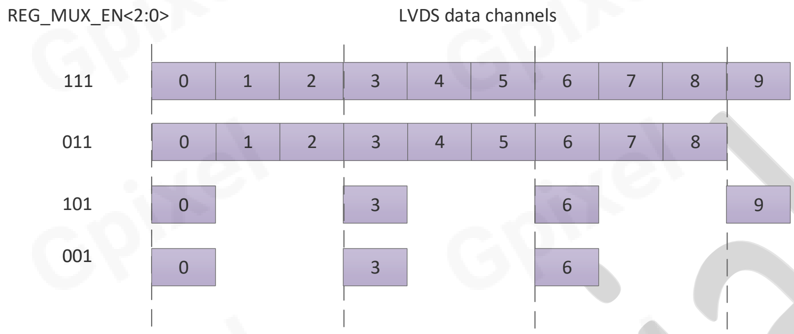


Figure 50: LVDS channel multiplexing

Table 18: Data LVDS channel multiplexing register setting

Register address (H)	Bit	Register name	Description	Define
33	6:4	REG_MUX_EN<2:0>	LVDS channel multiplexing	011: 9 data LVDS channel (12-bit HDR default) 001: 3 data LVDS channel (14-bit STD default)

It is not allowed to use higher number of LVDS outputs than the default setting stated in this document. If other LVDS channel multiplexing is preferred, please contact Gpixel Inc. first.

Data Receiving

In digital control signals, the control signal SYNC is X-axis synchronization signal. The following figure illustrates the data receiving principle. As mentioned in "LVDS Training" section, a delay time T_{delay} (T_{delay_x} for different channels) should be taken into account. Compare to the rising edge of SYNC signal, the first effective column data has a delay T_{SYNC} which is calculated as:

$$T_{SYNC} = T_{del\_var} + 7 \times T_{CLK\_SEQ}$$

T_{del_var} is not a fixed value, and is equal to T_{delay_x} or ($T_{delay\_x} \pm N \times T_{CLK\_SEQ}$ / ADC_Depth). T_{CLK_SEQ} is period of one CLK_SEQ cycle. In each line time, one LVDS channel will always output N_{line_time} pixel data, with the data sequence shown in Figure 51 and Figure 52 respectively. After the SYNC pulse, each channel will always output 4 SYNC code (SOF or SOL) data first, followed by M valid data. M depends on the LVDS channel multiplexing. M will be 444 and 636 respectively with 9 LVDS channels and 1332 and 1524 respectively with 3 LVDS channels.

Note:
Since T_{del_var} is not a fixed number, so it is recommended to do a word correction in each line-time.

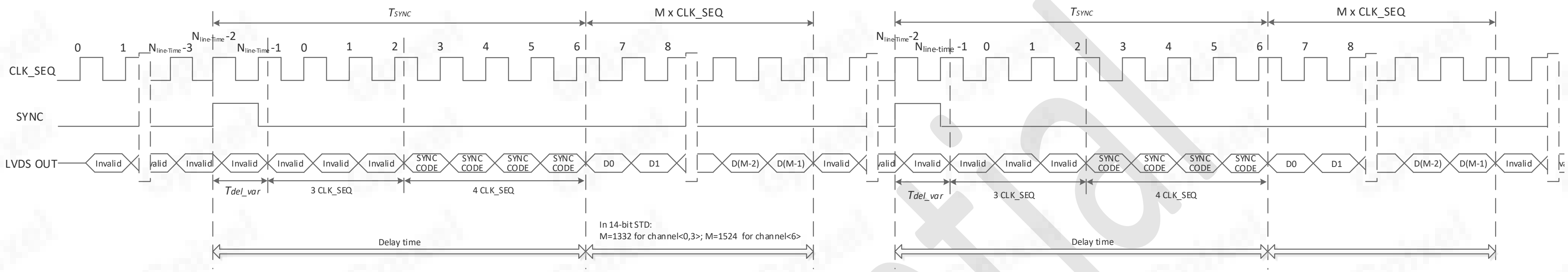


Figure 51: Data receiving for GSENSE1517BSI in 14-bit STD mode

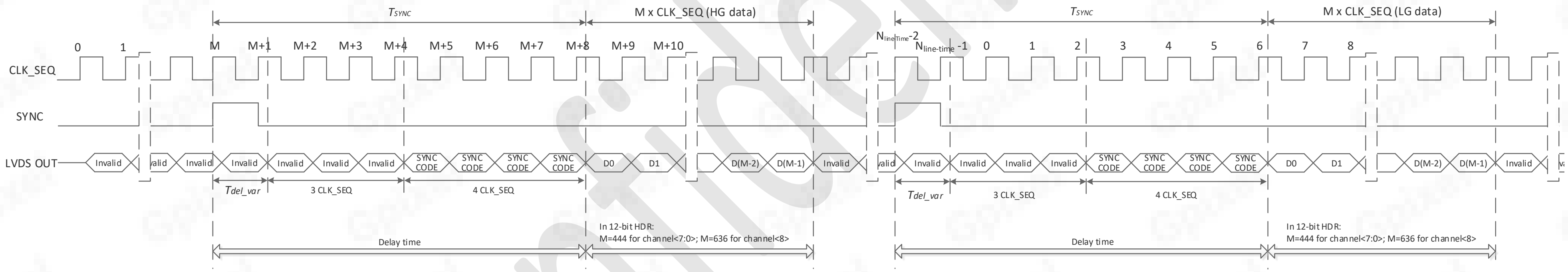


Figure 52: Data receiving for GSENSE1517BSI in 12-bit HDR mode

Image Data Output Format

SYNC Code

Sync code is added in the image sensor output to indicate the correct pixel data. The Sync code is always 4-word in serial. There are four types of Sync codes used in GSENSE1517BSI sensor. They are listed below.

Table 19: Types of SYNC codes in STD mode

Sync code	Description
SOF	Start of Frame: Beginning of Image
SOL	Start of Line : Beginning of horizontal line

Table 20: Types of SYNC codes in HDR mode

Sync code	Description
SOF	Start of Frame: Beginning of Image
SOLH	Start of HG Line: Beginning of high gain horizontal line
SOLL	Start of LG Line: Beginning of low gain horizontal line

Table 21: Details of the SYNC codes in 14-bit STD mode

Sync code	First word	Second word	Third word	Fourth word
	14-bit	14-bit	14-bit	14-bit
SOF	3FFFh	0000h	0000h	0801h
SOL	3FFFh	0000h	0000h	0AB1h

Table 22: Details of the SYNC codes in 12-bit HDR mode

Sync code	First word	Second word	Third word	Fourth word
	12-bit	12-bit	12-bit	12-bit
SOF	FFFh	000h	000h	801h
SOLH	FFFh	000h	000h	AB1h
SOLL	FFFh	000h	000h	EB1h

The following figure shows the data format of the image.

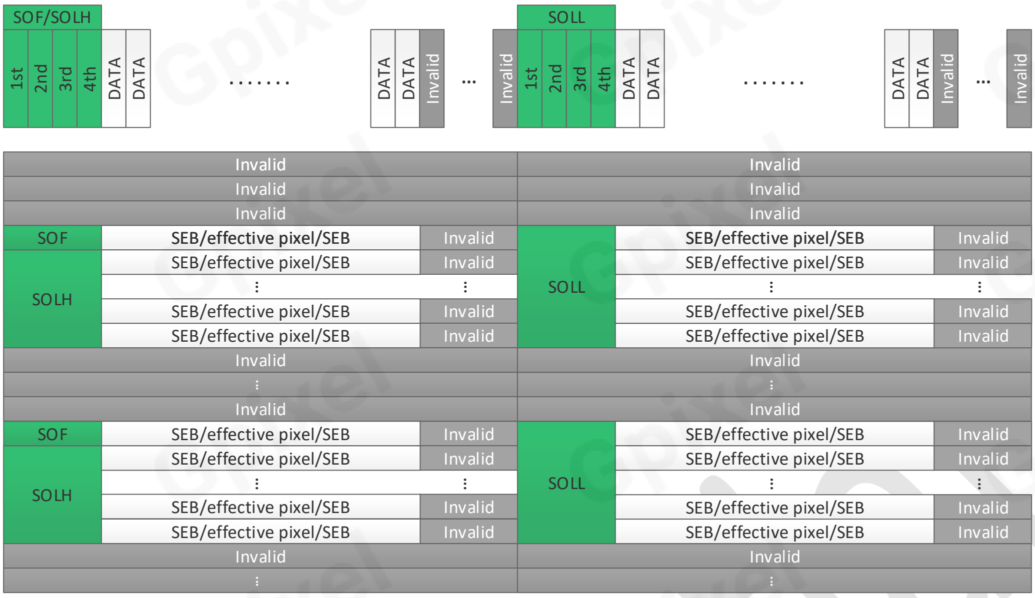


Figure 53: 12-bit HDR image data output format with SYNC Code

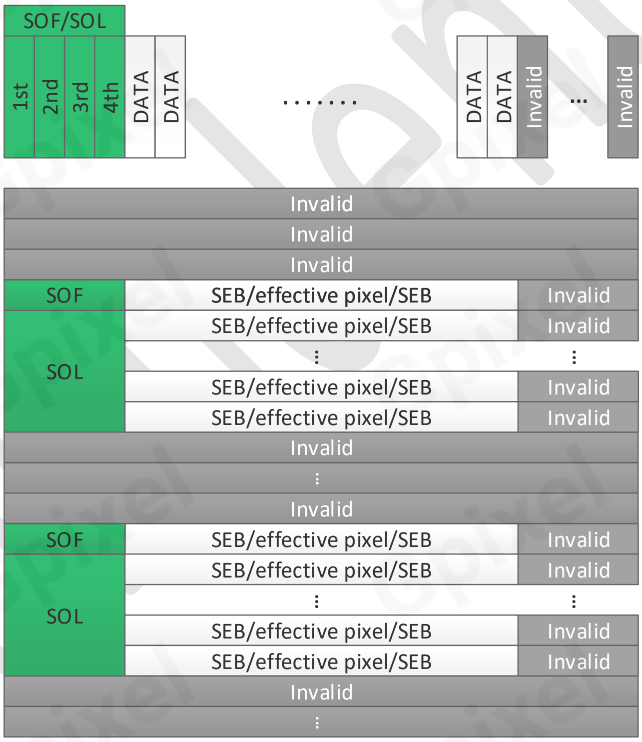


Figure 54: 14-bit STD image data output format with SYNC Code

DATA Output Format

Because of pipeline readout structure, there is a delay between the pixel reading and data output

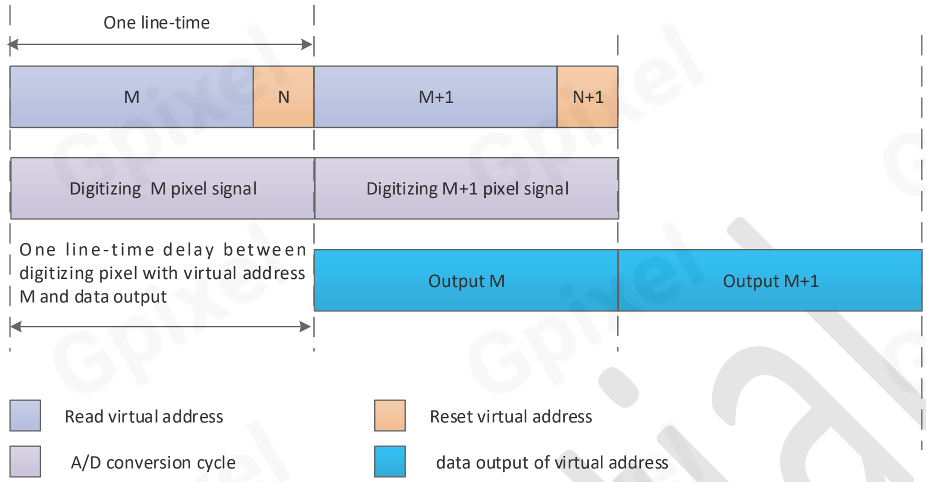


Figure 55: Pipeline readout structure

The data output formats in 12-bit HDR and 14-bit STD modes are shown in Figure 56 and Figure 57.

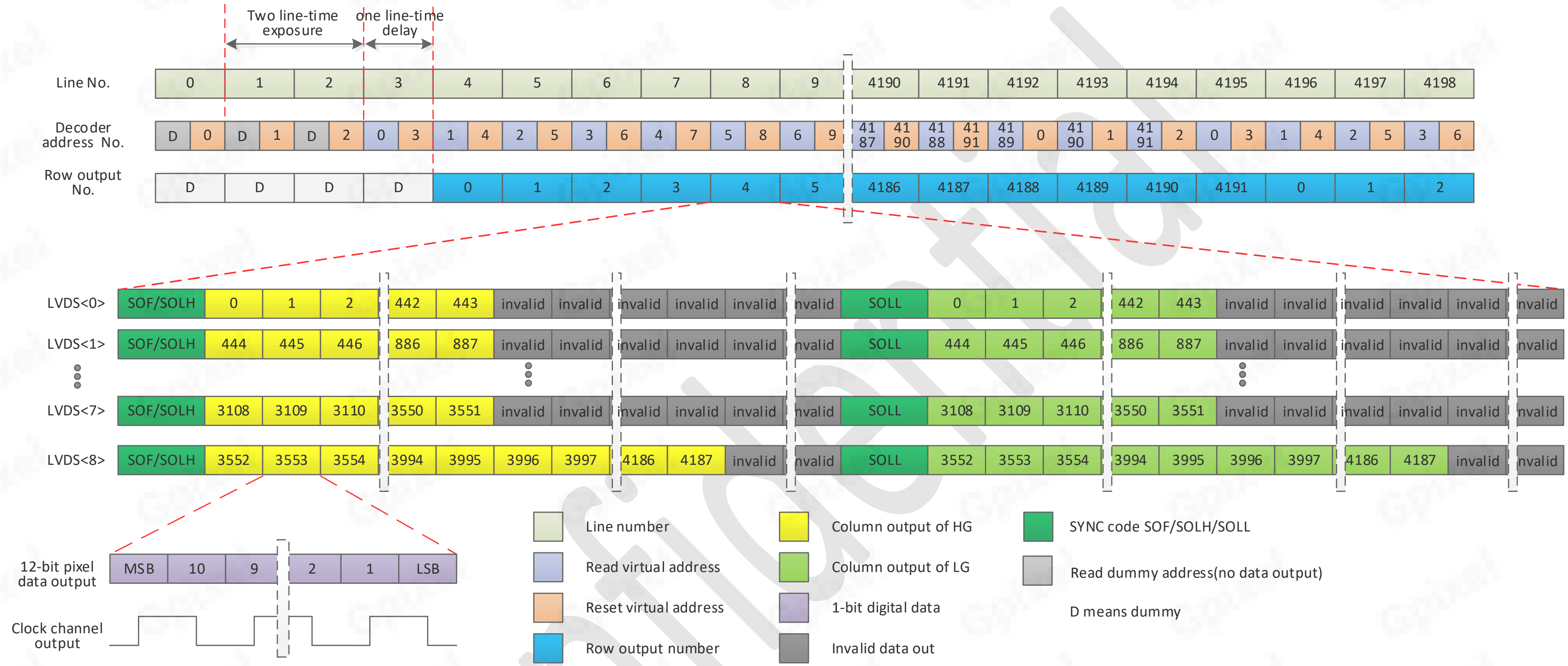


Figure 56: 12-bit HDR data output format

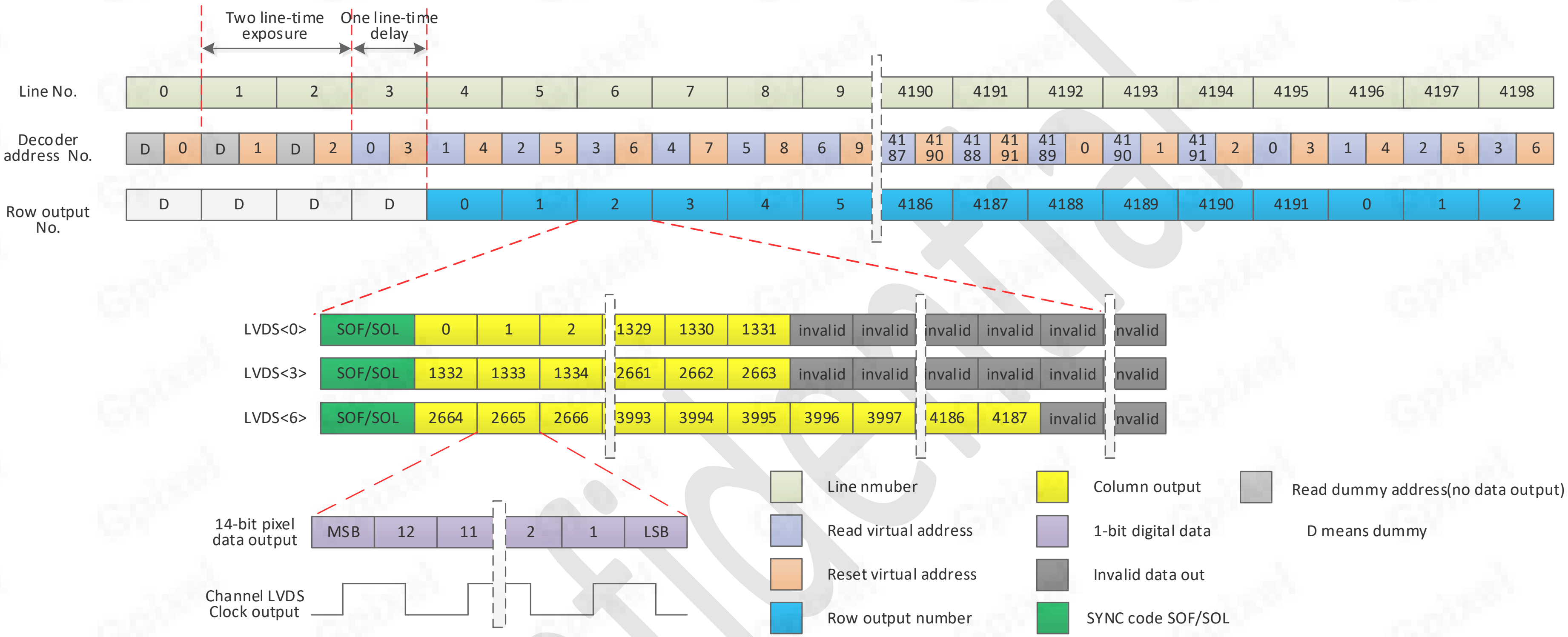


Figure 57: 14-bit STD data output format

Description of Various Functions

Black Level Adjustment

The black level of the image will be determined by several parameters, such as:

1. Voltage reference VRAMP_INIT, VRAMP_PC, VBG, VREF, VPCH, VPCL.
2. Register setting of REG_DARK_OFFSET_HG<17:0>and REG_DARK_OFFSET_LG <17:0>.
3. Others: the temperature variation may cause the black level drift.

REG_DARK_OFFSET_HG<17:0> is used for black level adjustment of data from 12-bit HDR HG and 14-bit STD readout. REG_DARK_OFFSET_LG<17:0> is used for black level adjustment of data from 12-bit HDR LG readout.

Table 23: Registers for dark offset setting of GSENSE1517BSI

Address (H)	Bit	Register name	Description
32	1:0	REG_DARK_OFFSET_HG <17:0>	Used to adjust the black level of HG image in 12-bit HDR mode. Used to adjust the black level in 14-bit STD mode.
31	7:0		
30	7:0		
36	7:0	REG_DARK_OFFSET_LG <17:0>	Used to adjust the black level of LG image in 12-bit HDR mode.
35	7:0		
34	7:6		

Windowing Operation

The device does not support multi-window operations, only single-window in vertical direction is supported. Horizontal window operation is not supported.

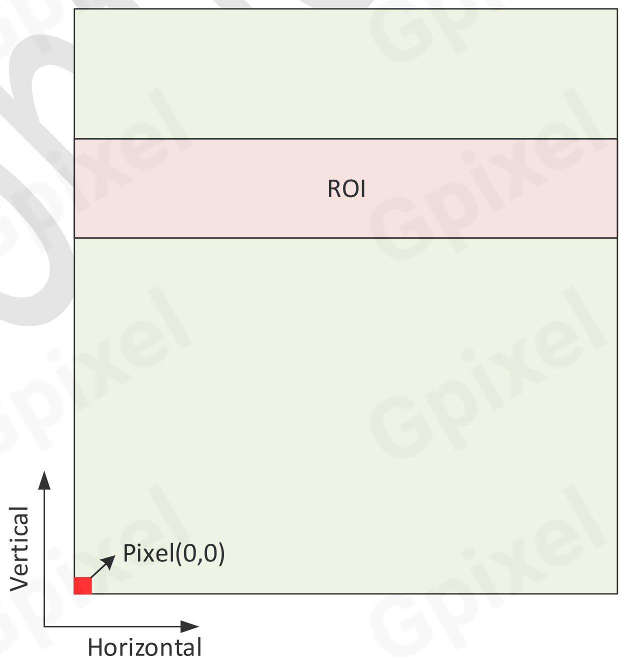


Figure 58: window operation

Test Image

GSENSE1517BSI can be configured to output a test image for users to debug the surrounding system. The related registers to configure are described in Table 24. The data of pixel(X,Y) is calculated by:

$$\text{Part N in 14-bit STD mode: } DN_{test\_image} = 1 + (X - 1332 \times N + Y)\%DN_{max} \quad 0 \leqslant N \leqslant 2$$

$$\text{Part N in 12-bit HDR LG: } DN_{test\_image} = 2 + (X - 444 \times N + 2 \times Y)\%DN_{max} \quad 0 \leqslant N \leqslant 8$$

$$\text{Part N in 12-bit HDR HG: } DN_{test\_image} = 1 + (X - 444 \times N + 2 \times Y)\%DN_{max} \quad 0 \leqslant N \leqslant 8$$

The test image for 12-bit HDR and 14-bit STD are shown in Figure 59 and Figure 60 respectively.

Table 24 Registers setting for GSENSE1517BSI to output test image

Address (H)	Bit	Name	Description
34	4	REG_TEST_DATA_EN	1: Test image out 0: Image capture

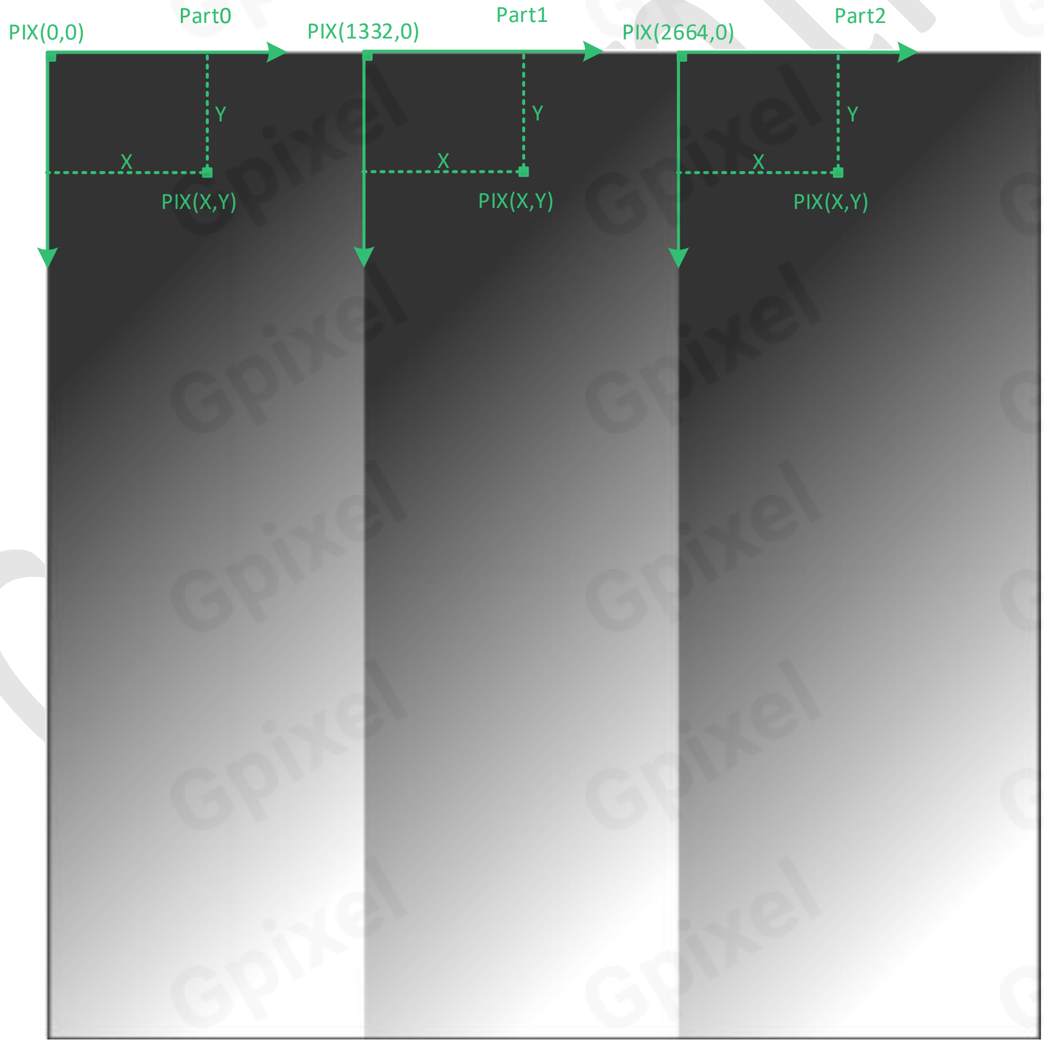


Figure 59: Test image output of 14-bit STD mode

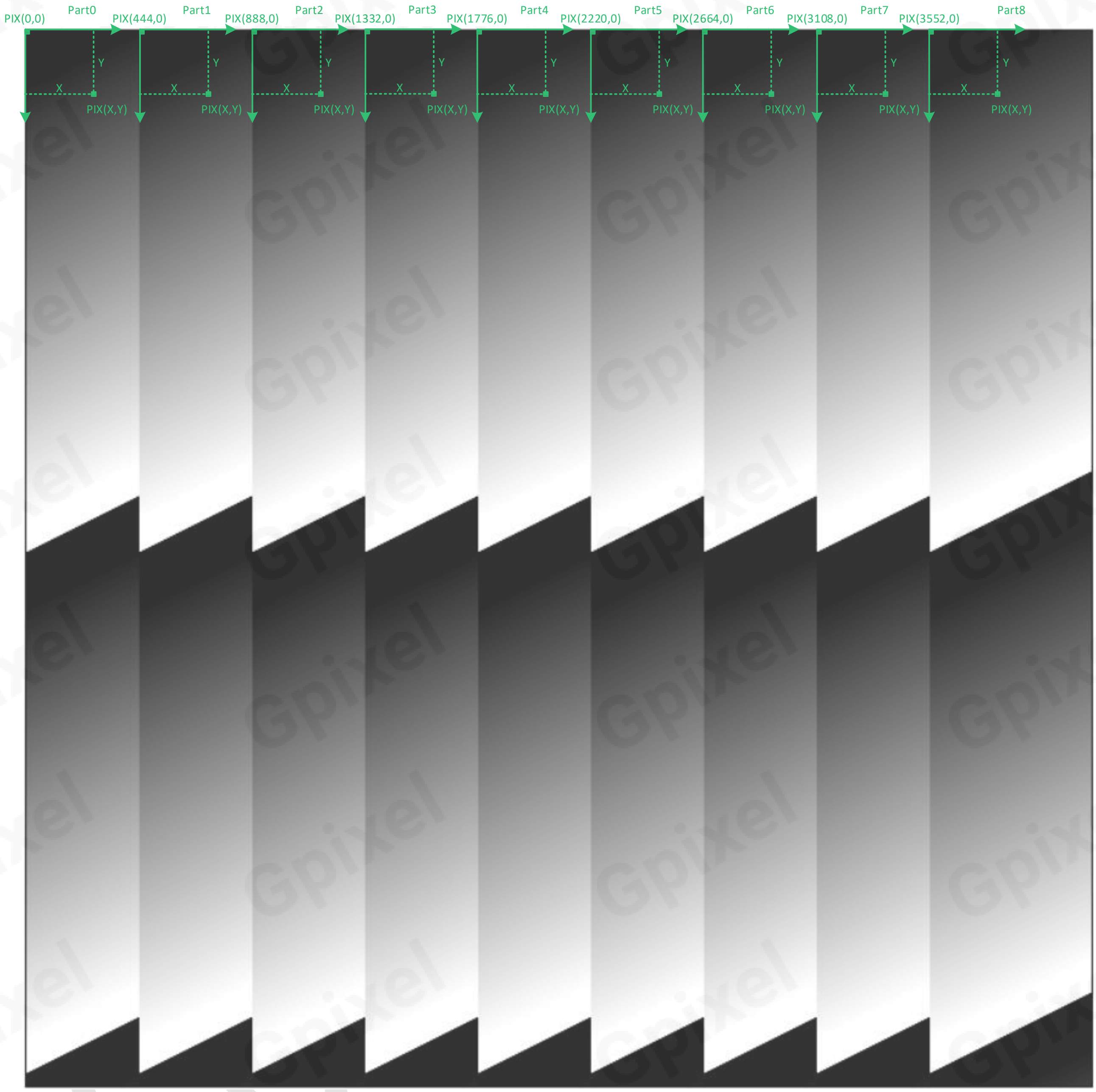


Figure 60: Test image output of 12-bit HDR mode

Blemish Specification

All Blemish Specification in this chapter is preliminary versions, it is subject to change without notice.

Test Mode

GSENSE1517BSI sensor outgoing test is performed with the 12bit HDR operation mode. The defect limits apply to Area of 4116(H) x4100(V) pixel array shown in figure below, **the orange area**.

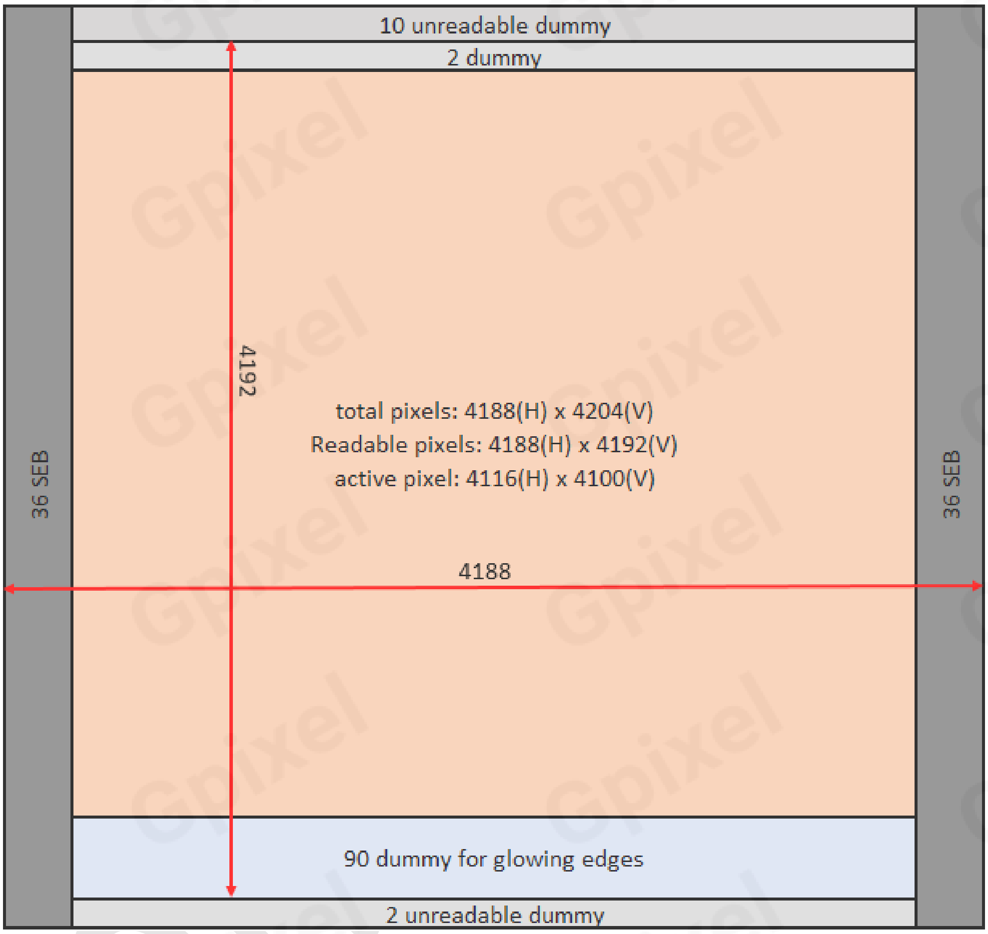


Figure 61: Defect Controlled Region

Outgoing Test Image

The test images are generated using evaluation system with a light source of uniformity better than 96%. Sensor is configured in 12-bit HDR mode with default settings of datasheet.

Table 25: Image definition

Image Level	Definition
Dark	In dark environment and with exposure time of 1 line time, 2 images are grabbed and averaged, for HG and LG channel individually.
Grey	2 images at half-saturation are grabbed and averaged, for HG and LG channel individually.
Saturation	2 images at saturation are grabbed and averaged, for LG channel only.
Half-saturation images	The half-saturation image for HG channel is constructed by subtracting the HG Dark image from the HG Grey image.

	The half-saturation image for LG channel is constructed by subtracting the LG Dark image from the LG Grey image.
Saturation image	The saturation image is constructed by subtracting the LG Dark image from the LG Saturation image.

Defect Definitions

Table 26 below describes the definition of blemish.

Table 26: Blemish definition

Defect Name	Description
Defect pixel in Half-saturation image	Any pixel deviates more than 30% from the mean value of the Half-saturation image (either HG or LG channel).
Defect pixel in Saturation image	Any pixel deviates more than 30% from the mean value of the Saturation image (LG channel only).
Total Defect Pixel	The total number of non-overlapping defect pixels in Half-saturation image and Saturation image.
Defect Row	Any row with its mean value deviating more than 10% from the mean value of the Half-saturation image (either HG or LG channel); Any row with its mean value deviating more than 10% from Saturation image of the LG channel; Or a row with more than 150 Defect pixels;
Defect Column	Any column with its mean value deviating more than 10% from the mean value of the Half-saturation image(either HG or LG channel); Any column with its mean value deviating more than 10% from Saturation image of the LG channel; Or a column with more than 150 Defect pixels.

Defect Limits

Maximum allowed defect numbers are indicated below.

Table 27: Defect limits

Item	Demo Grade
Total Defect Pixel	800
Total Defect Column and Defect Row	2

Any Defects on the glass lid are excluded.

Storage Condition, Handling and Soldering

CMOS image sensors require delicate handling, ESD can cause sensor malfunction or even damages; many external elements, like dust, oil and scratches etc.,can degrade sensor's performance. To reduce the risk of sensor damages, here Gpixel presents general guidelines and basic techniques for CMOS image sensor proper handling. Evidence of incorrect handling will invalidate the sensor warranty.

ESD Damage Prevention

To prevent ESD damage, Gpixel recommends following general procedures:

- Ensure the ESD protective working area is properly setup.
- Make sure the operator is grounded prior handling the sensors.
- Using ESD safe gloves to handle sensors.
- Ground all tools and mechanical components that come in contact with the sensors.
- Gpixel also recommends using antistatic solutions and air ionizers to prevent static charge buildup.

Storage Condition

GSENSE1517BSI sensors are recommend to store in a temperature and humidity controlled environment, preferable in a N2 filled cabinet; or keep the sensor in vacuum sealed ESD bags.

Soldering Guideline

Gpixel recommends using sockets for BSI sensors camera assembly. If socket is not applicable, manual soldering can be used. The BSI sensors may be damaged in reflow soldering or wave soldering process.

When a soldering iron is used for manually soldering the sensors to a through-hole board, conditions as below should be followed:

Profile Feature	Recommended Condition
Solder iron tip temperature	Max 350°C
Pin temperature	Max 270°C
Time	typical 2s-3s, max 3s

Please avoid global heating on ceramic packages during soldering.

Note:
Gpixel recommends customers to purchase engineering samples or mechanical samples to setup a suitable soldering process prior apply the soldering process for mass production. The soldering profiles Gpixel provides is only for reference purpose. Gpixel does not take responsibility if the sensor is damaged in the soldering processes.

Temperature Change and Vacuum

BSI sensor surface is delicate, to avoid large thermal shock and vacuum induced stress, following measures shall be followed.

- For cooling application, it is recommended that the maximal cooling rate below 3 degree/minute.
- Vacuum compatibility, it is compatible at 0.01 mTorr for vacuum application.

Product Order Information

For ordering information, please see below table for details.

Table 28 Ordering information

Product number	Description	Marking Code
GSENSE1517BSI-ABM-NFN-NND	BSI Image Sensor, monochrome without microlens on die. Silicon carbide with 144-pin Al_2O_3 IPGA ceramic package Without glass lid. Demo Grade	GSENSE1517BSI-A5LV Serial number

Note:

1. Engineering sample sensor is available based on request. Change product number's last digit to E for engineering sample ordering.
2. Engineering sample sensor is defined as sensor with normal functionality but failed blemish defect limit.

Rights

Contact

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